

# COMPAL CONFIDENTIAL

MODEL NAME : ZBU10

PCB NO : LA-A961P

BOM P/N : 4319RL31L01

GPIO MAP: 3.6C

## Goliad MLK 14" UMA

Broadwell U

2014-10-07

REV : 1.0(A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

VPRO@ : VPRO Component

NVPRO@ : NVPRO Component

Layout Dell logo



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REV: X02  
PWB: 407FT

MB PCB @

Part Number	Description
DAA0084000	PCB DVM LA-A961P REV0 UMA MB WITH DOCKING

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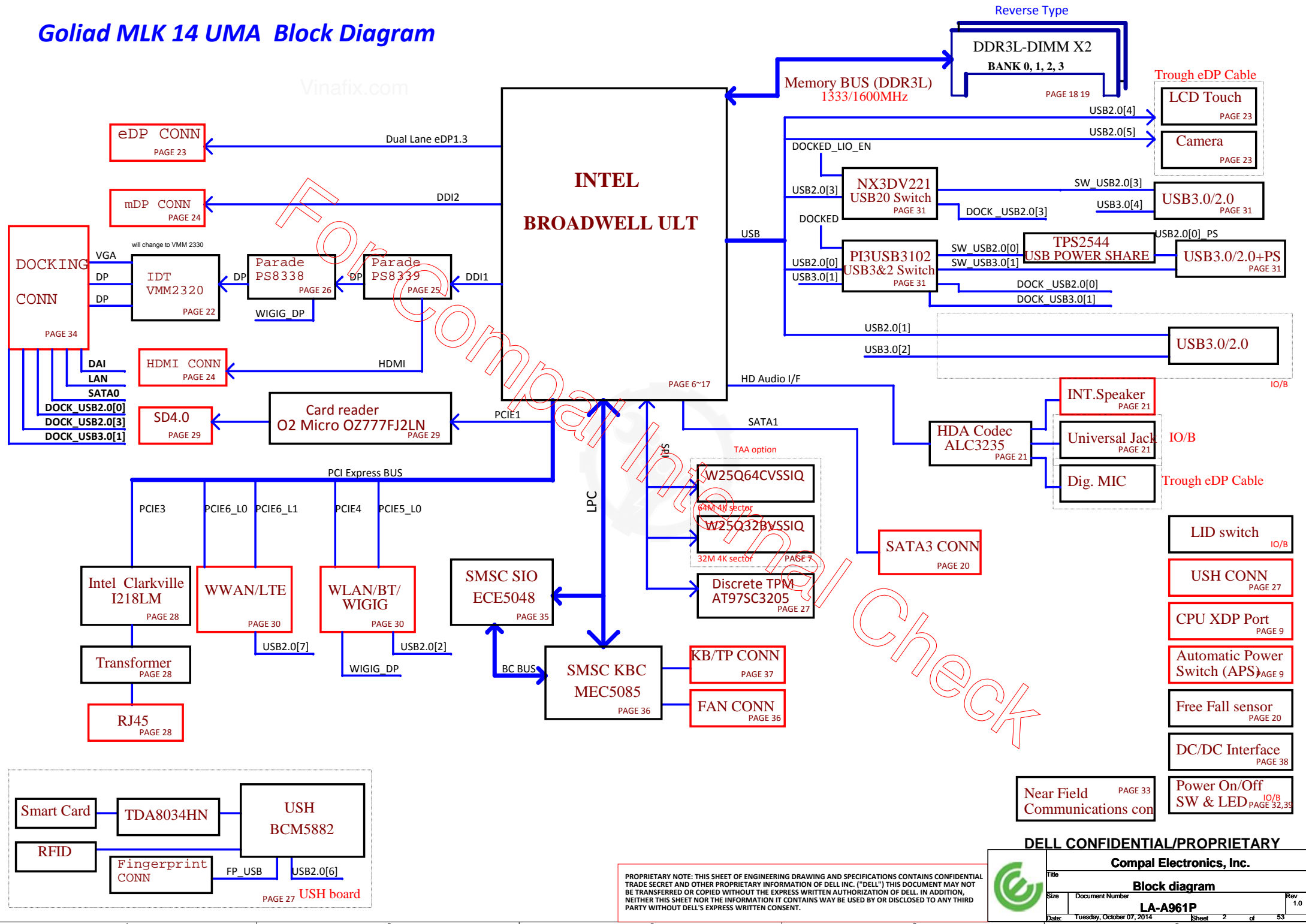


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Cover Sheet

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# Goliad MLK 14 UMA Block Diagram



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Block diagram			
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## POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

## PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M (M-OFF)	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN - JNGFF1
PCIE 5			WiGig - JNGFF1
PCIE 6		SATA 3	HCA & SATA Cache - JNGFF2
		SATA 2	SATA Cache - JNGFF2
		SATA 1	JSATA1
		SATA 0	JDOCK1

BDW ULT	USB PORT#	DESTINATION
	0	JUSB1 or DOCK1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2 or DOCK2
	4	Touch Screen
	5	CAMERA
	6	USH
	7	WWAN

USH	0	BIO
	1	NA

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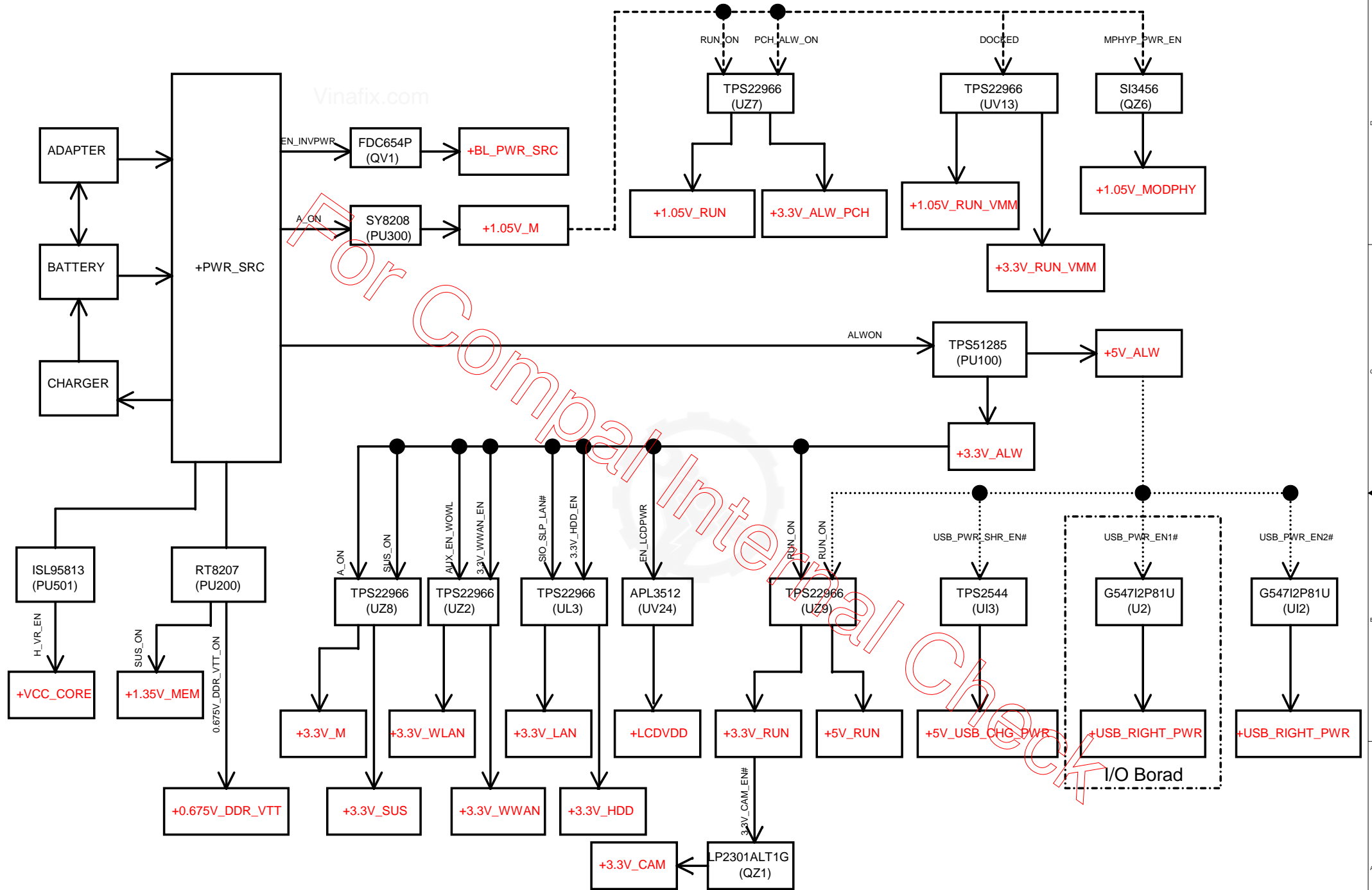
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Port assignment

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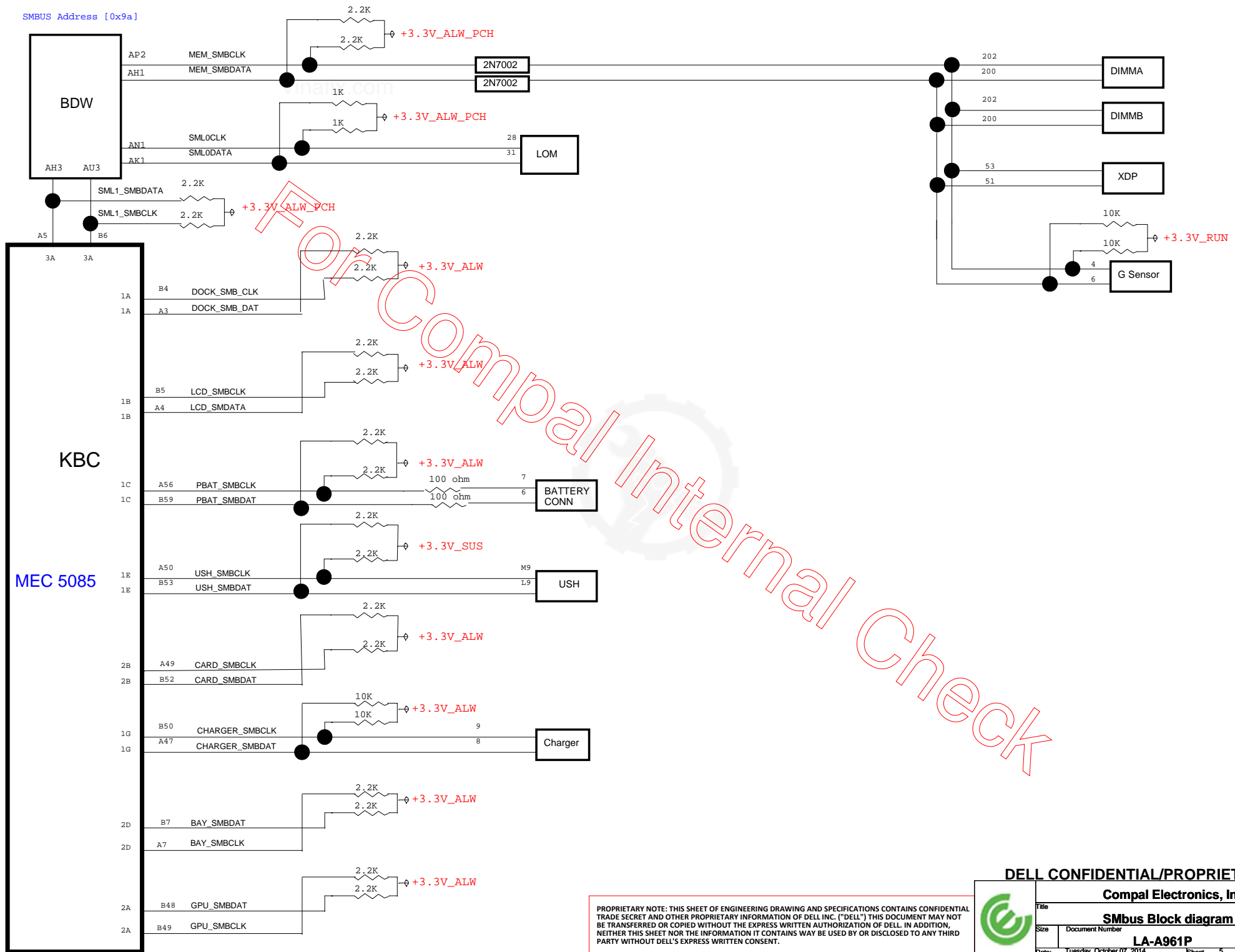
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Power rails

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SMBUS Address [0x9a]



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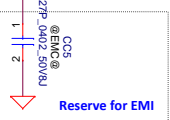
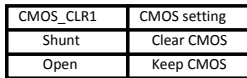
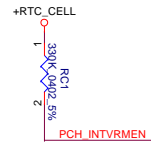


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SMBus Block diagram			
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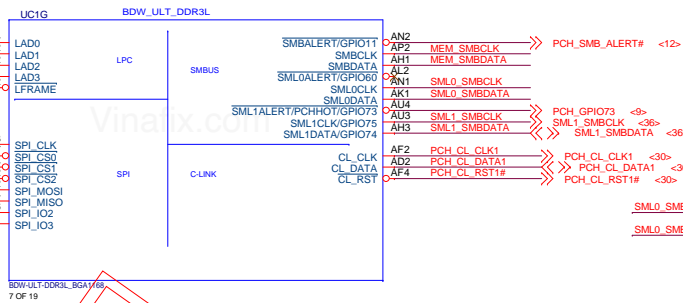
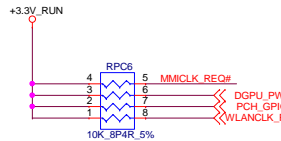
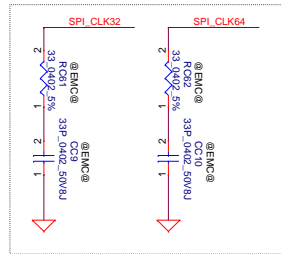
SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0
E-Dock	mSATA	G12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	mSATA	G12 Entry	NA	NA
E-Dock	mSATA	G14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG
E-Dock	HDD	G14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	mSATA	G14D_En	NA	M2 3030 WIGIG
NA	HDD	G14U_En	NA	NA

**contact to WLAN**

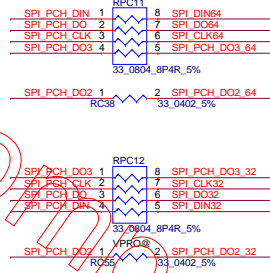


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#### SOFTWARE TAA



#### PCIECLK for UMA

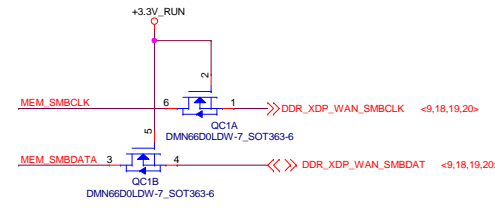
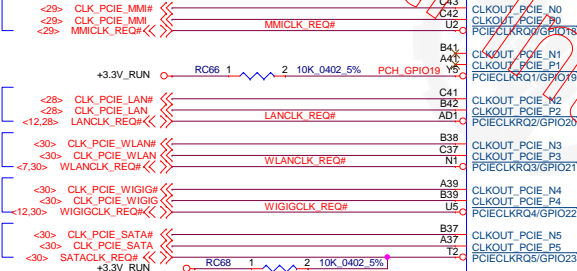
MMI --->

10/100/1G LAN --->

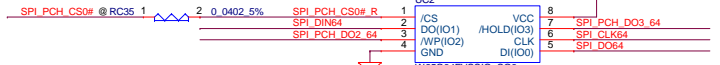
WLAN (NGFF1) --->

WIGIG (NGFF1) --->

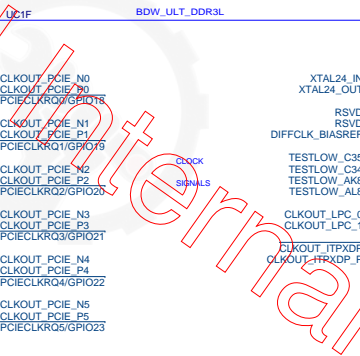
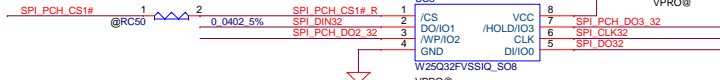
HCA/PCie cache (NGFF2) --->



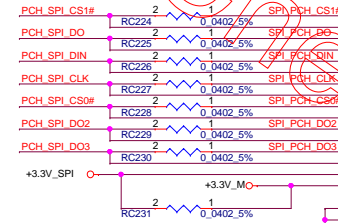
#### 64Mb Flash ROM



#### 32Mb Flash ROM

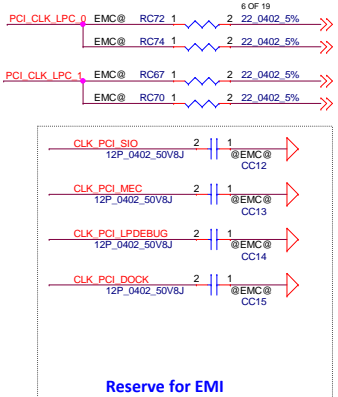


from CPU to SPI ROM



support SPI TPM		support LPC TPM	
LPC_0	LPC_1	LPC_0	LPC_1
SIO	DOCK	CLKBUFF	DOCK
MEC	DEBUG	SIO	DEBUG
		MEC	
		TPM	

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
G12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
G14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
G14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
G14U_En	SD card	NA	LOM	WLAN	WIGIG	NA



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CPU (2/12)

LA-A961P

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EDP\_COMP 24.9\_0402 1% 2 1 RC133 +VCCIOA\_OUT

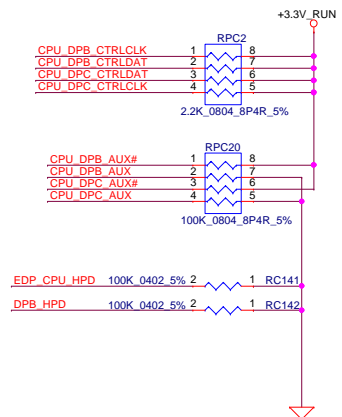
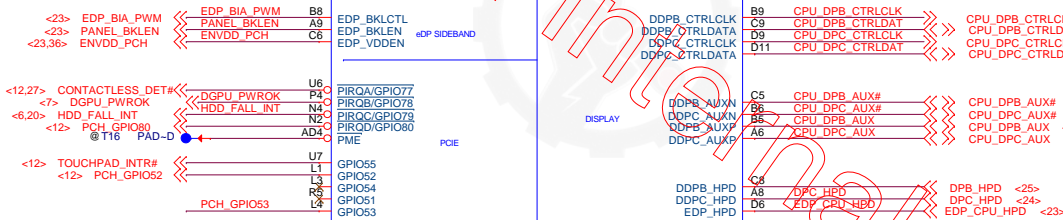
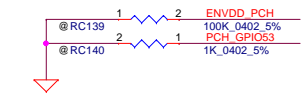
+3.3V\_RUN

5 4  
6 3  
7 2  
8 1

RPC15

10K 8P4R\_5%

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CPUSB# <12>  
USH\_DET# <12,27>  
CAM\_MIC\_CBL\_DET# <12,23>

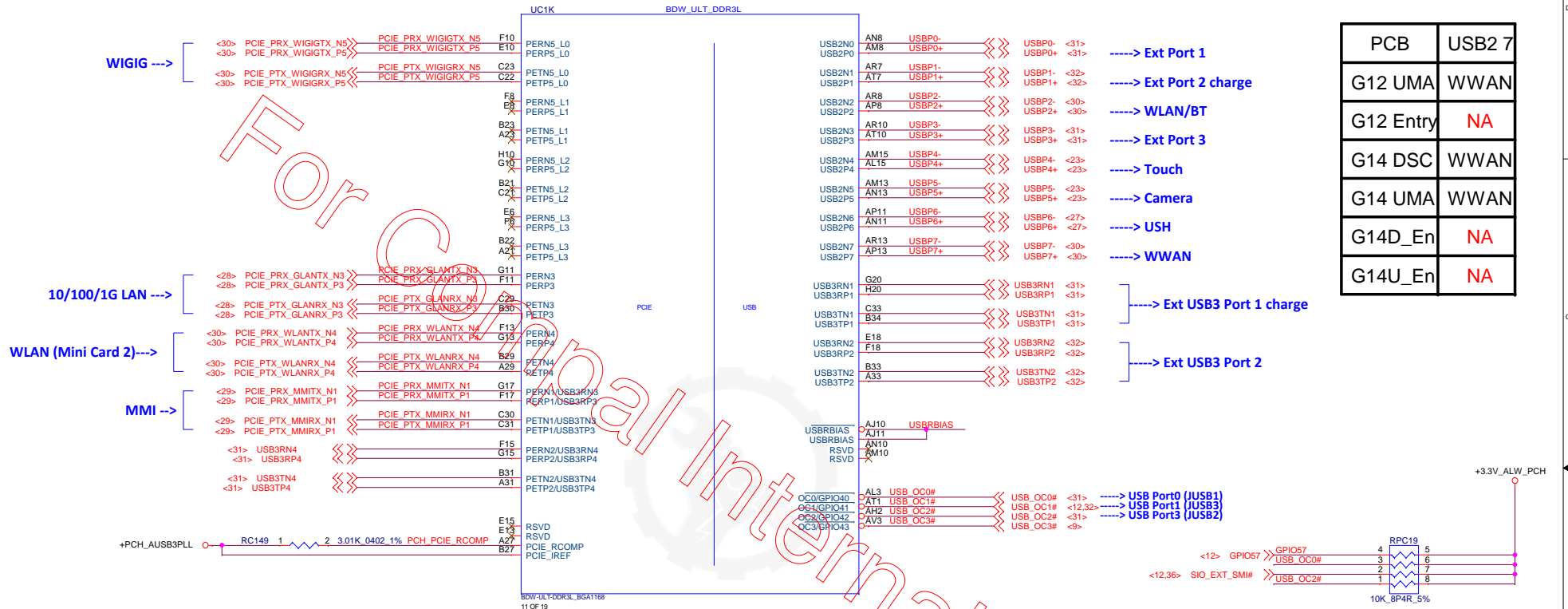


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## PCIE for UMA



PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
G12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
G14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
G14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
G14U_En	SD card	NA	LOM	WLAN	WIGIG	NA

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CPU (6/12)

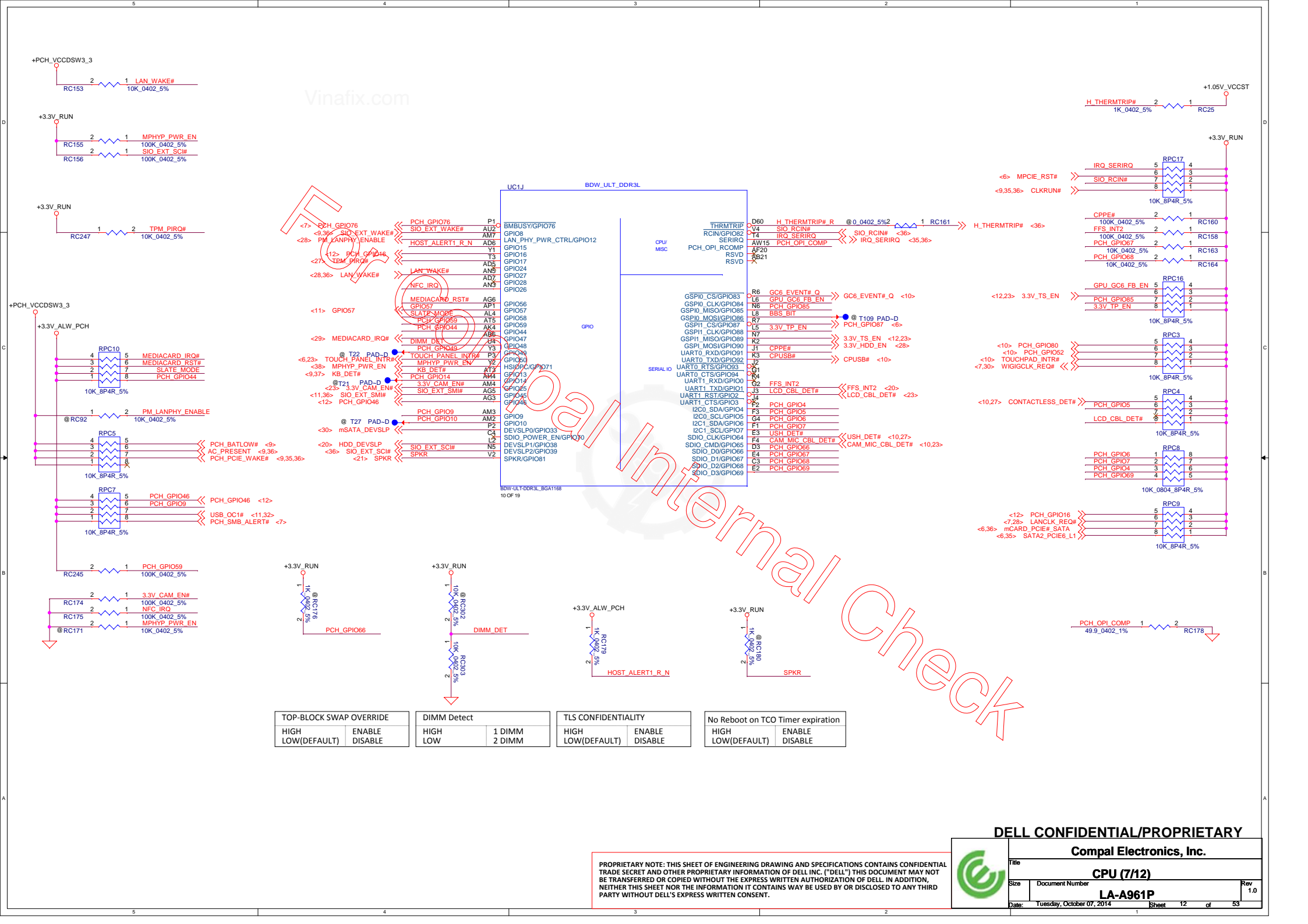
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TOP-BLOCK SWAP OVERRIDE	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

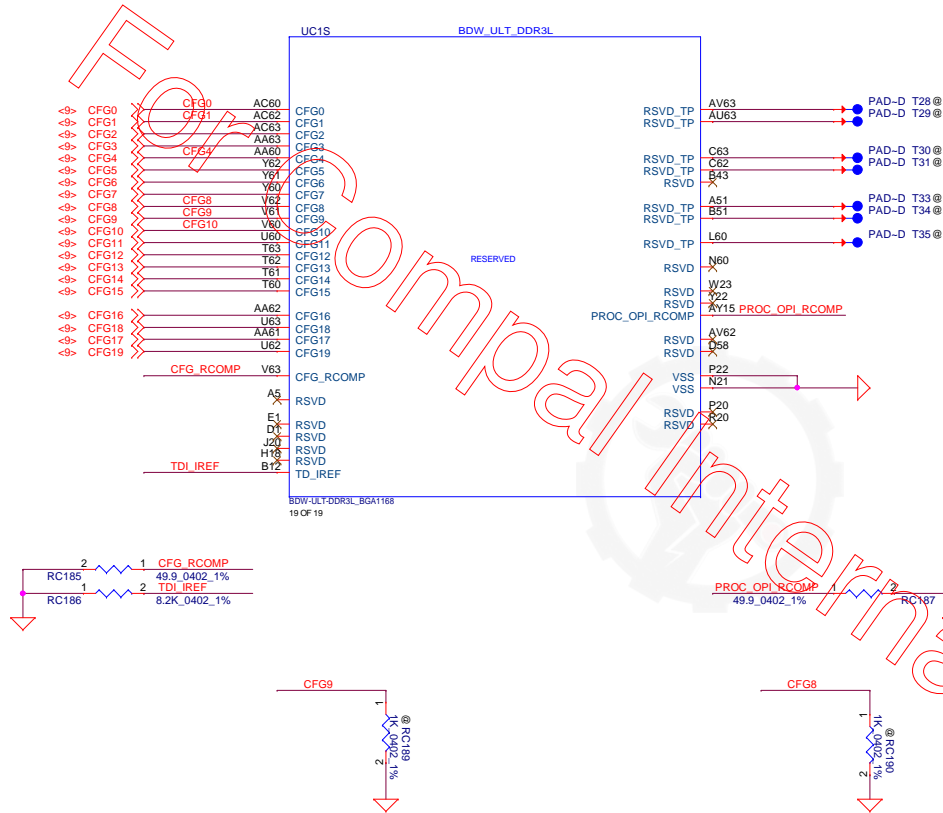
No Reboot on TCO Timer expiration	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE



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## CFG STRAPS for CPU



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0: Lane Reversed

PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0: Lane Reversed

SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0: No VR support SVID is present The chip will not generate (OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable (Default): Noa will be disable in locked units and enable in un-locked units 0: Disable Noa will be available pegrardless of the locking of the unit

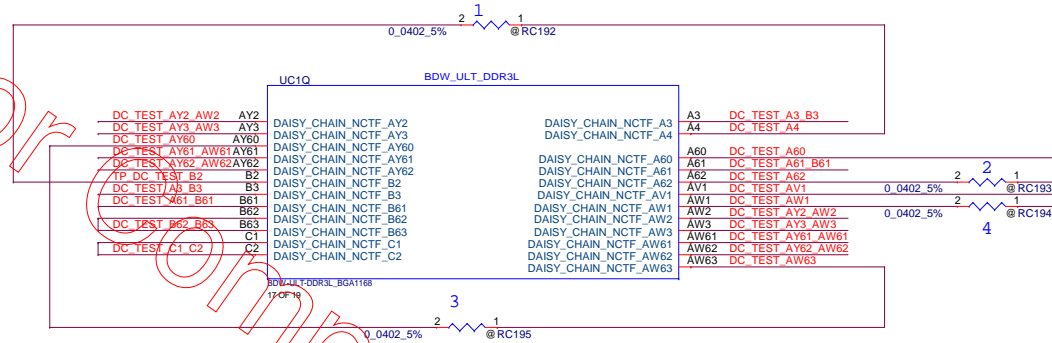
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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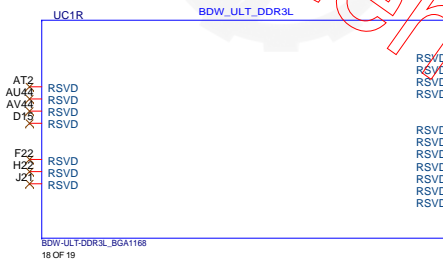


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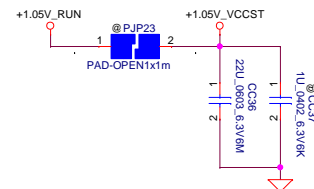
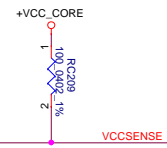
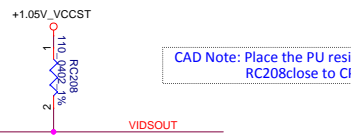
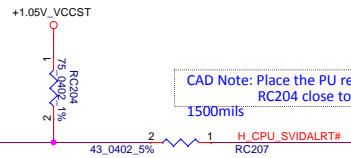
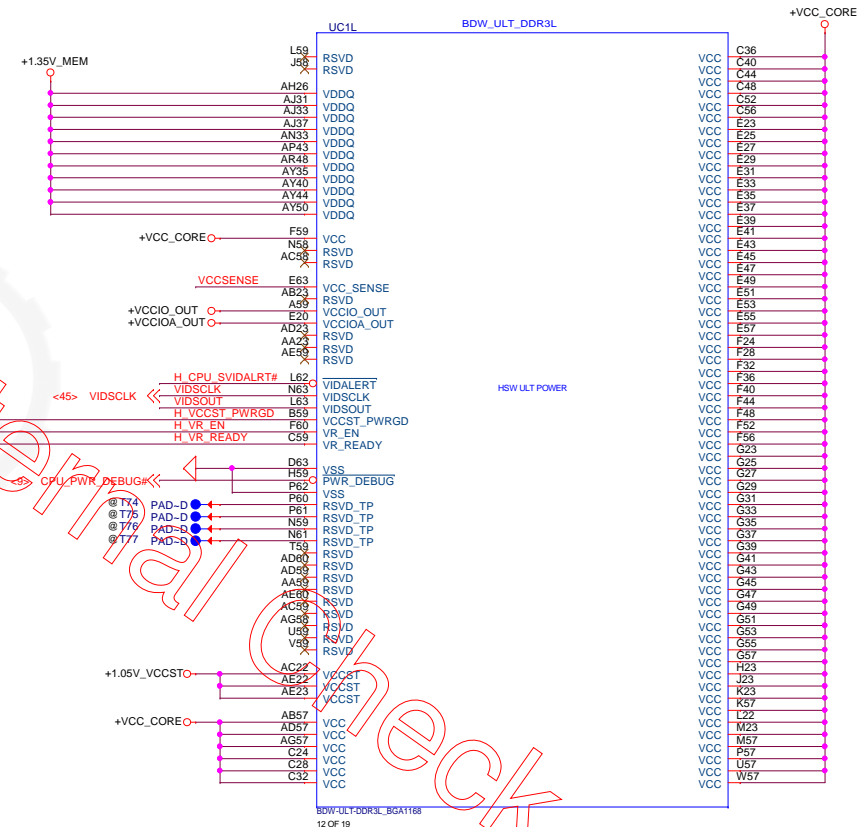
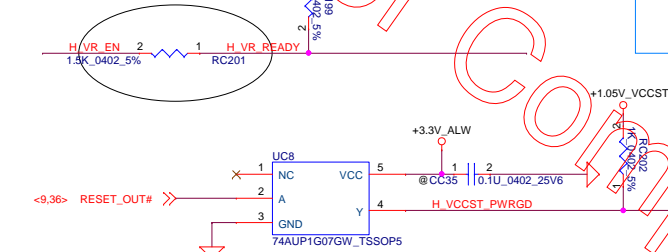
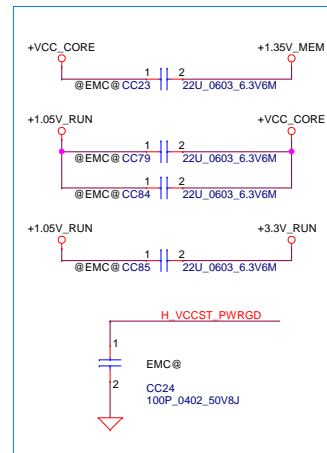
**Package Daisy Chain:**

- 1.B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4
- 2.A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
- 3.AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
- 4.AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1

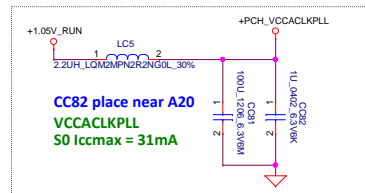
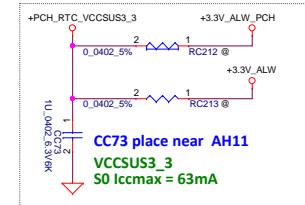
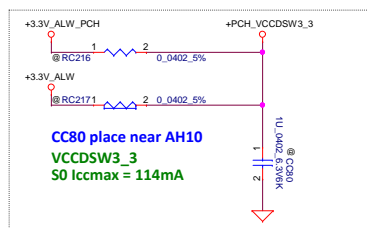
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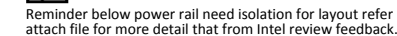
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Voltage Rail	Voltage (V)	S0 Iccmax Current (A) <sup>1</sup>	Sx Iccmax Current (A) <sup>2</sup>	Deep Sx Iccmax (A) <sup>3</sup>	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	0
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCCHDA	3.3	0.011	<1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1 <sup>4</sup>	1.05	0.109	0.014	0	0
DcpSus2 <sup>4</sup>	1.05	0.025	0.001	0	0
DcpSus3 <sup>4</sup>	1.05	0.010	0.003	0	0
DcpSus4 <sup>4</sup>	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 $\mu$ A See note 1, 2



### Power Rail Isolation

Voltage Supply	Interface (power rail isolation required)	PCH Pins sharing power rail
V1.05s	Core OP1 H9, L10, N0, P9, B10, B11, M9 USB2 CLKPLL CLK(A) CLK(B) CLK(C)	J11, H11, H15, AE8, AF22 AA21, W21 K9, L10, N0, P9, B10, B11, M9 AG16, AG17 A20 R21, T21 J18, K19 J17
V3.3a	GPIO RTC HDA	AC9, AA9, AE20, AE21 AH11 AH14
V3.3s	GPIO SDIO Thermal Sensor	VB, W9 UB, T9 K14, K16

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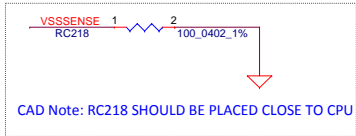
CPU (11/12)

LA 0061B

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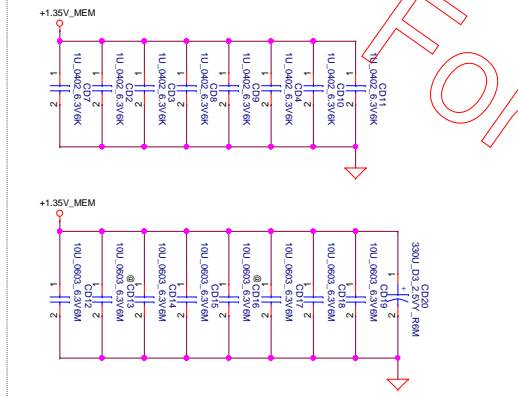


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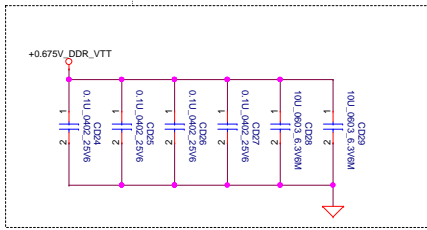
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<B> DDR\_A\_DQS# [0..7] <<>  
 <B> DDR\_A\_D [0..63] <<>  
 <B> DDR\_A\_DQS [0..7] <<>  
 <B> DDR\_A\_MA [0..15] <<>

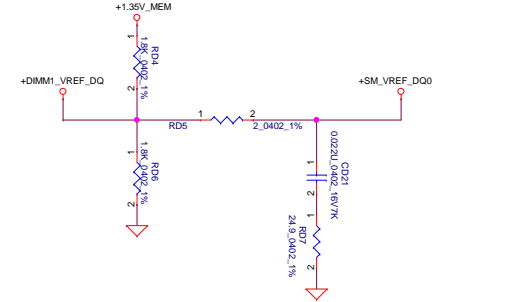
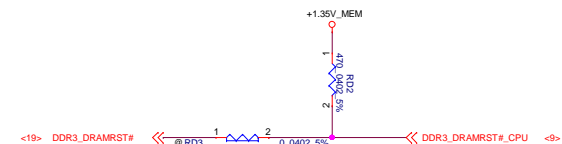
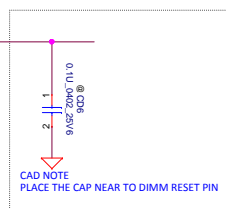
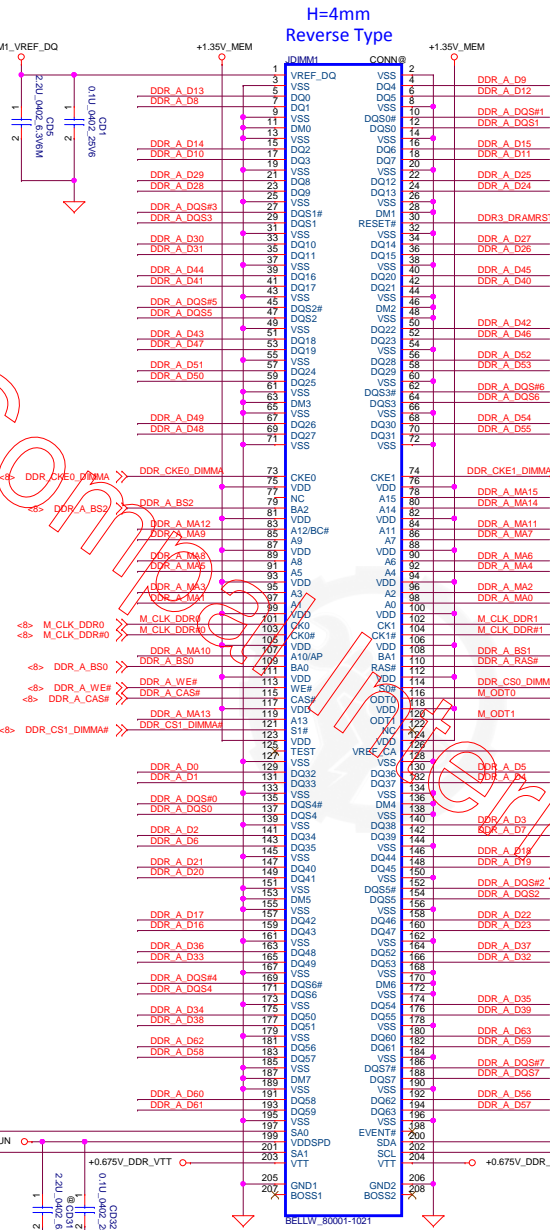
Layout Note:  
Place near JDIMM1



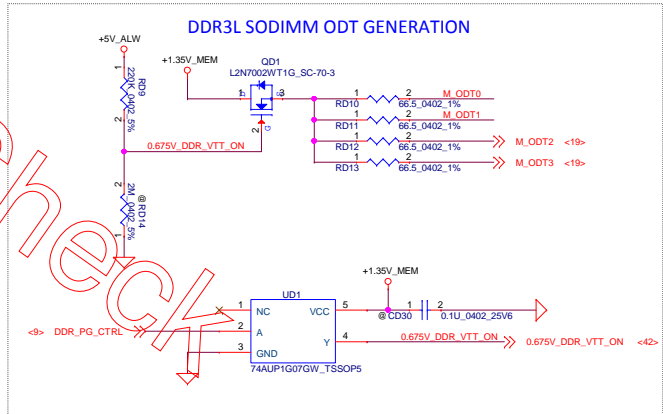
Layout Note:  
Place near JDIMM1.203,204



Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket



# DDR3L SODIMM ODT GENERATION



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DDR3L

LA-A961P

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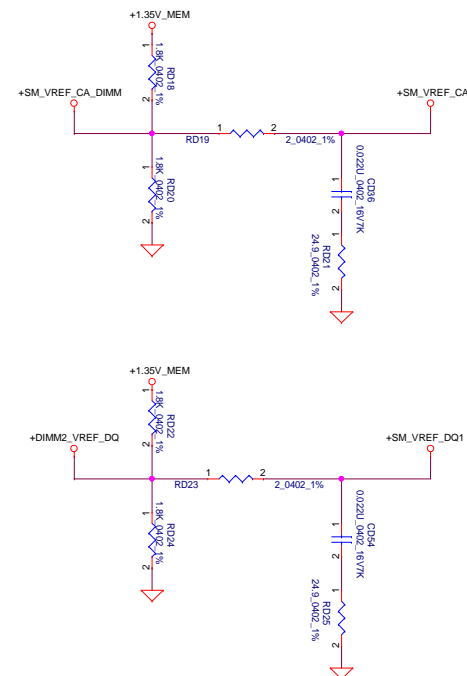
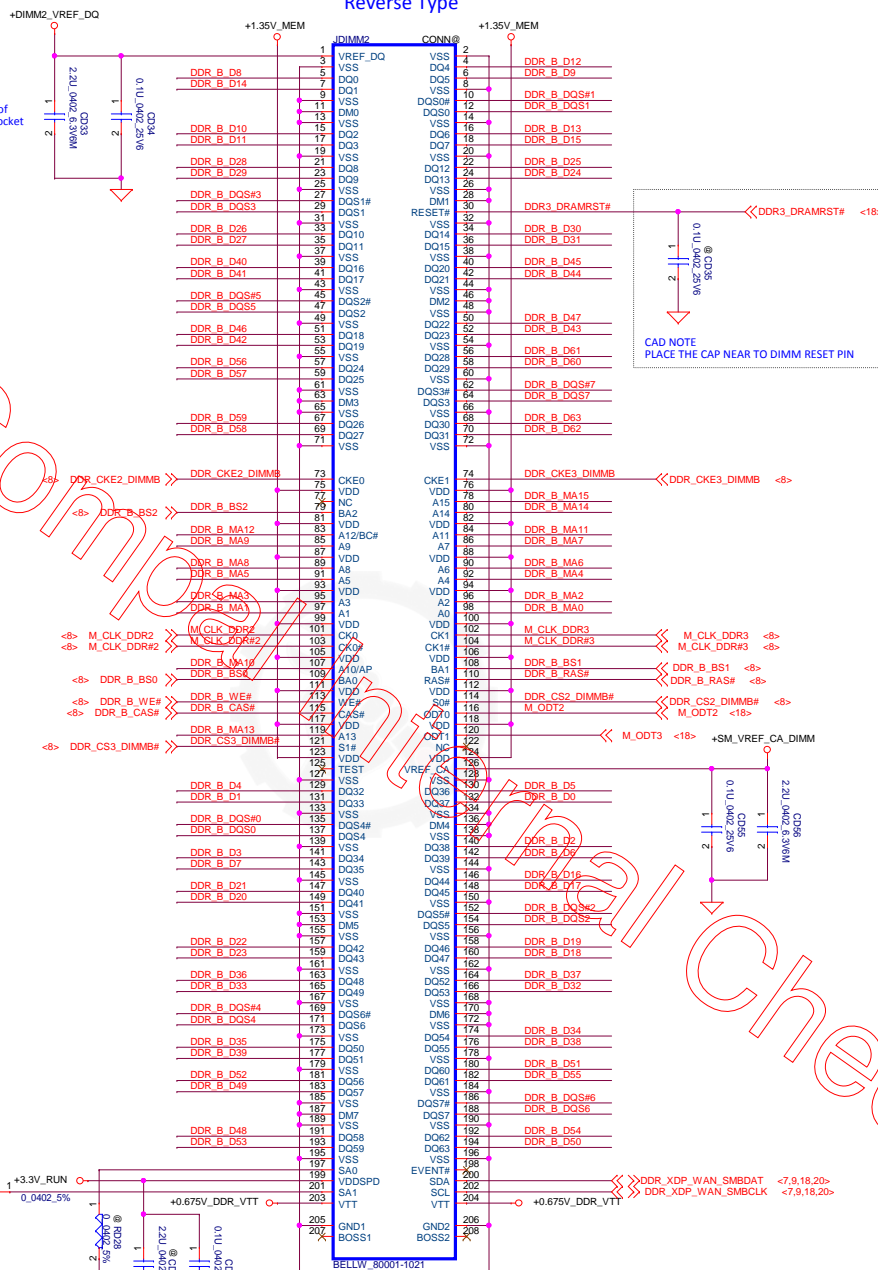
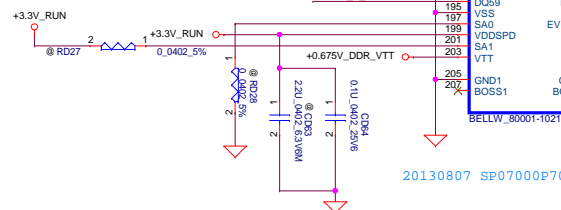
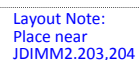


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1	LA-A961P	1.0

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Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket



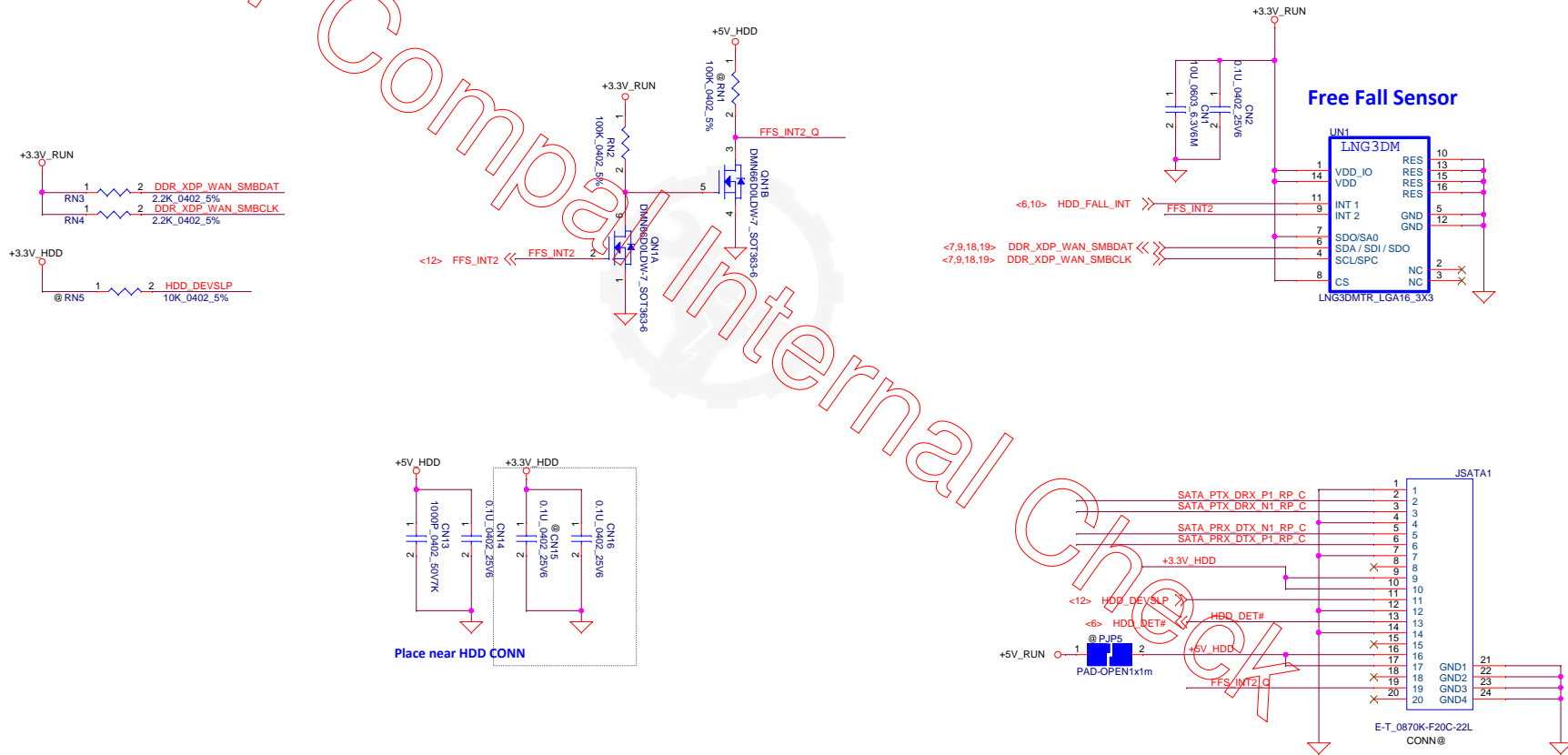
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<6> SATA_PTX_DRX_P1	>>	CN38 1	2	0.01U_0402_16V7K	SATA_PTX_DRX_P1_RP_C
<6> SATA_PTX_DRX_N1	>>	CN37 1	2	0.01U_0402_16V7K	SATA_PTX_DRX_N1_RP_C
<6> SATA_PRX_DTX_N1	>>	CN36 1	2	0.01U_0402_16V7K	SATA_PRX_DTX_N1_RP_C
<6> SATA_PRX_DTX_P1	>>	CN35 1	2	0.01U_0402_16V7K	SATA_PRX_DTX_P1_RP_C

## Bypass SATA Repeater



20131025 link SP01001GG00

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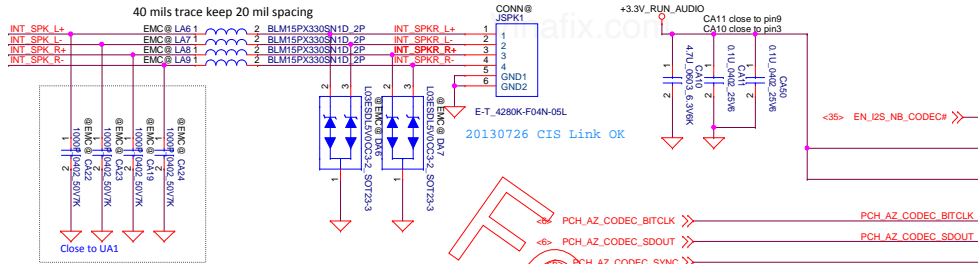
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HDD CONN			
Size	Document Number		Rev
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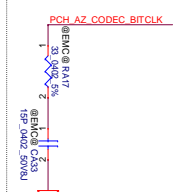
1W x 1ch, 4ohm (Transducer spec is 80hm/0.5Watt per unit, there are two transducer units in one speaker box)

## Internal Speakers Header

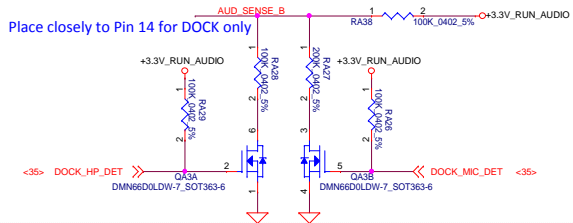
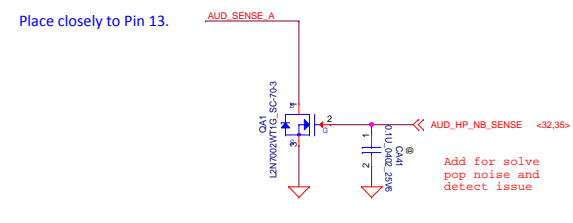
40 mils trace keep 20 mil spacing



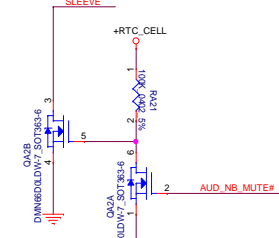
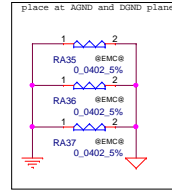
Close to UA1 pin6



Verb table configures as 1 JD mode with internal 47K pull high to save external R0M.

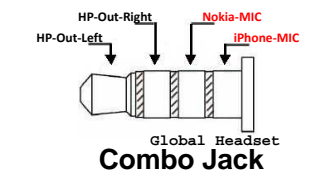
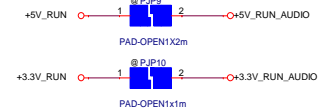
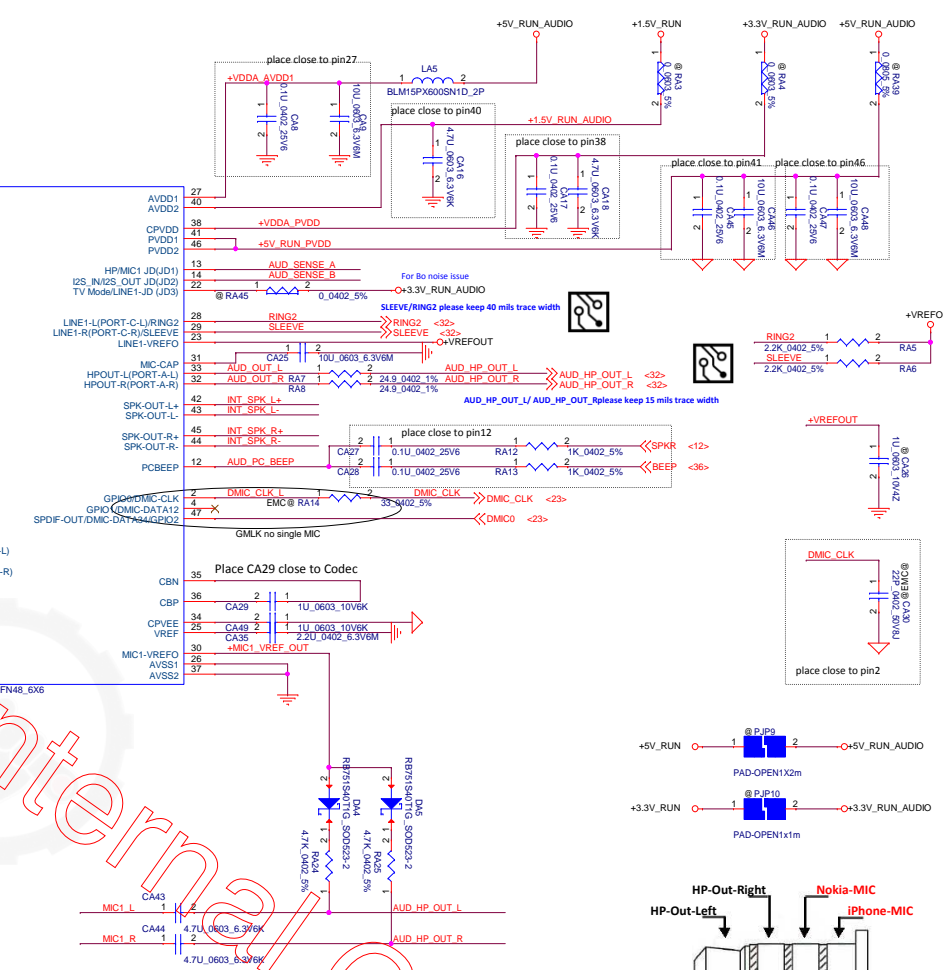


Digital Mic (Goliad MLK no single Mic)



Realtek feedback  
Prevent the Noise from Combo Jack  
while system entry into S3 / S4 / S5

Internal Check



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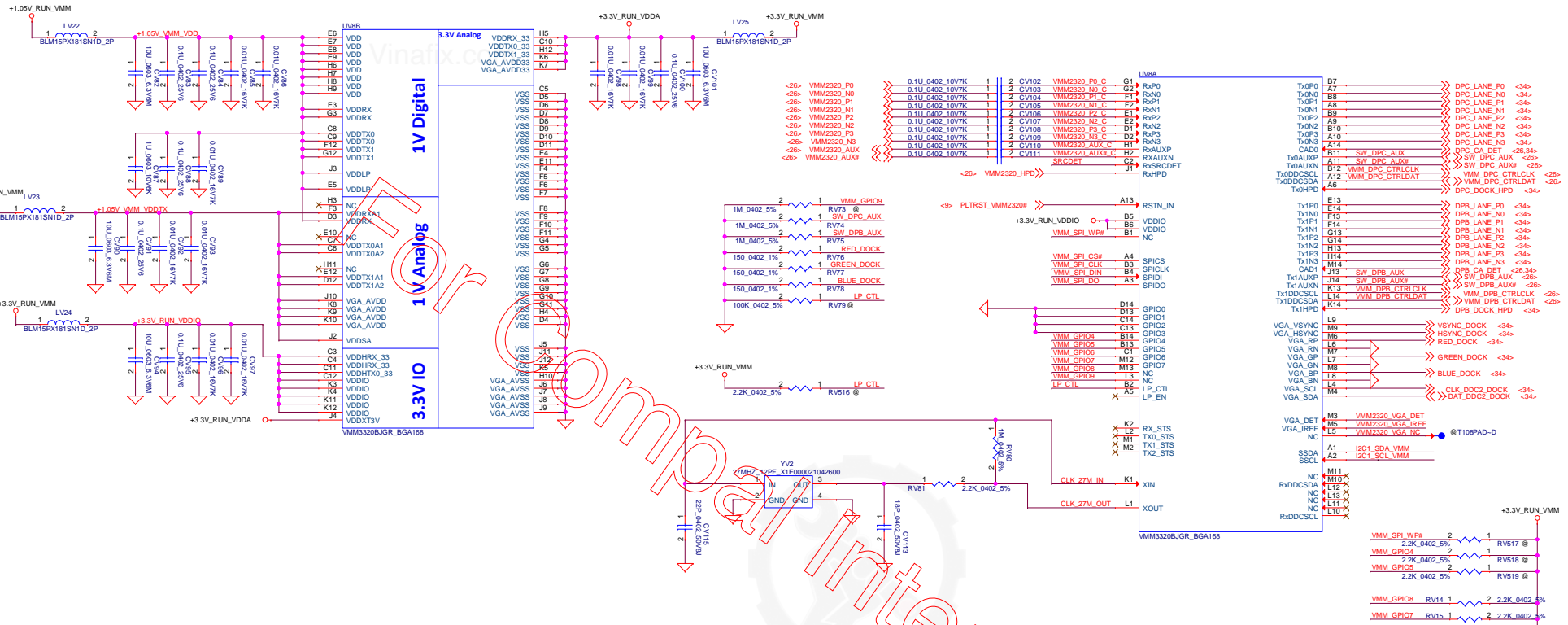
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Codec\_ALC3235

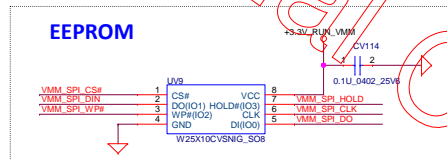
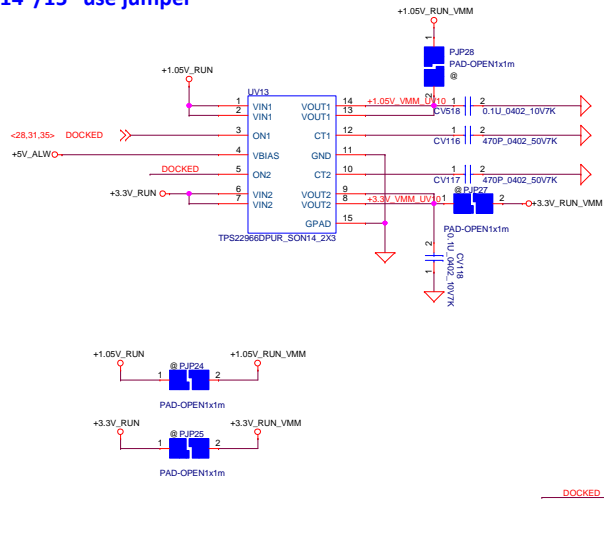
LA-A961P

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Goliad MLK should be use DOCKED to control TPS22966  
Huston 14"/15" use jumper



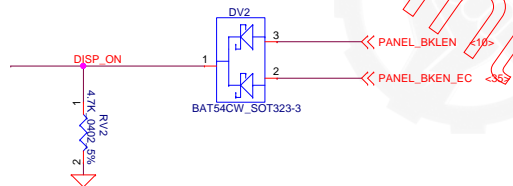
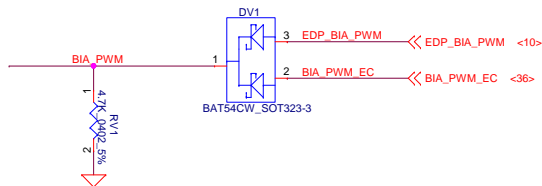
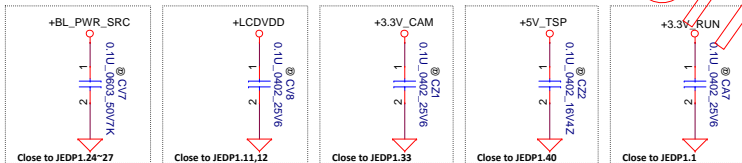
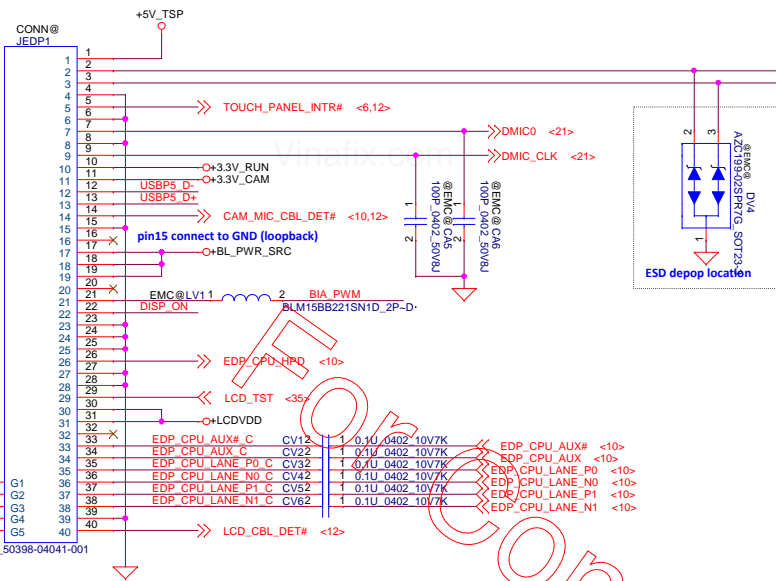
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Size	Document Number	LA-A961P		
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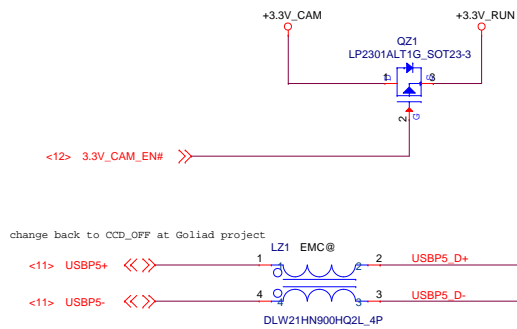
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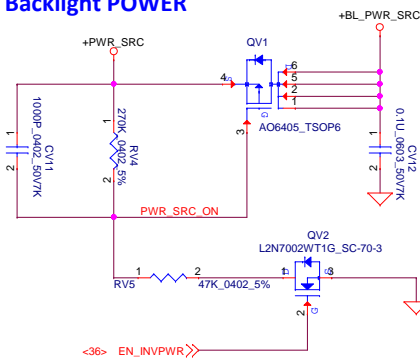
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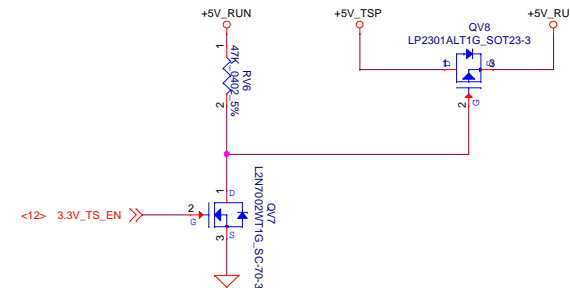
### WebCAM



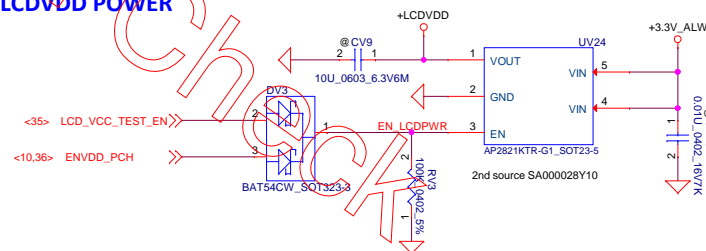
### Backlight POWER



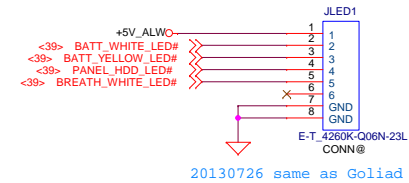
### For Touchscreen



### LCDVDD POWER



### LED CONN



20130726 same as Golliad

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eDP CONN & Touch screen

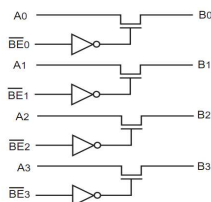
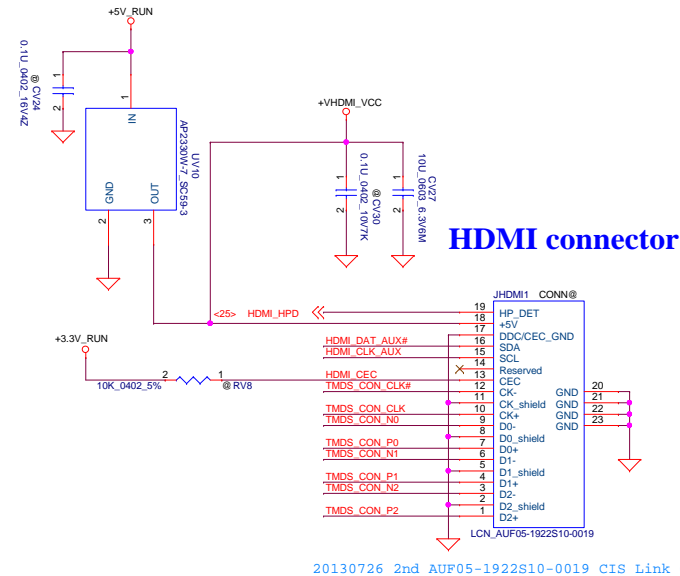
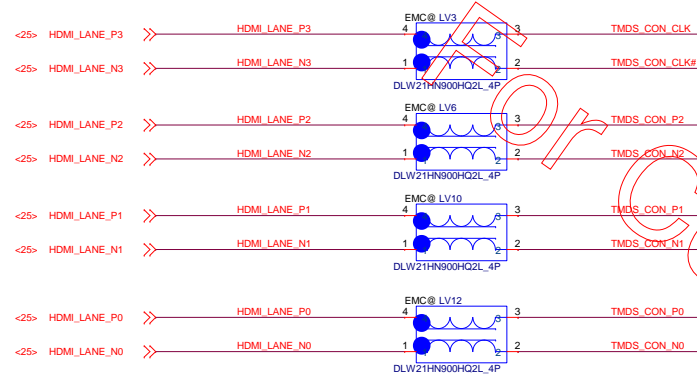
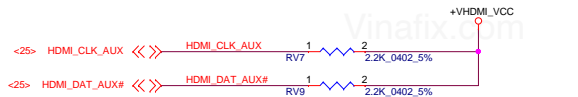
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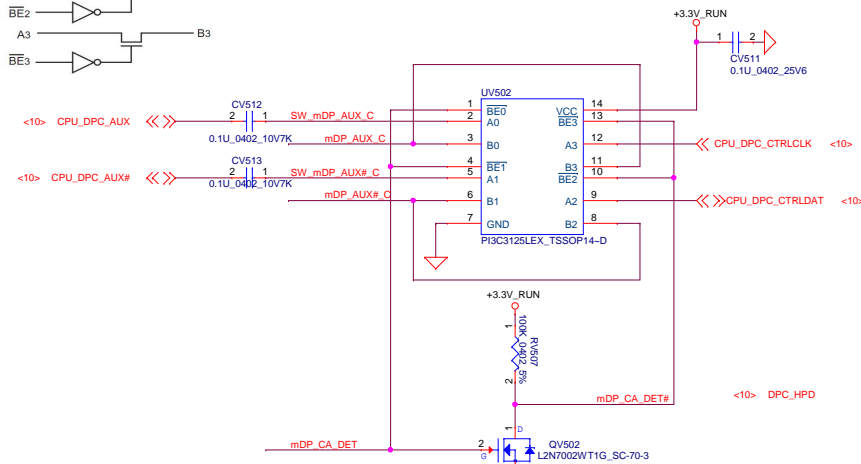
Tuesday, October 07, 2014

Rev 1.0

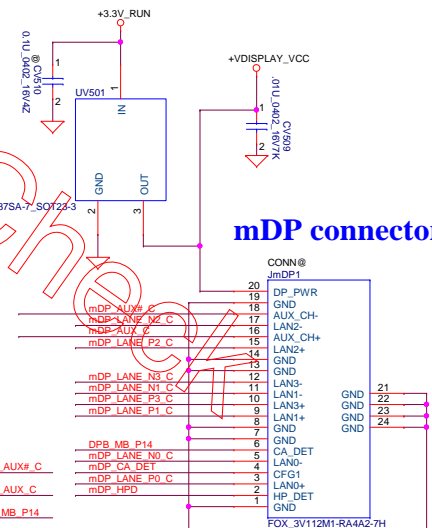
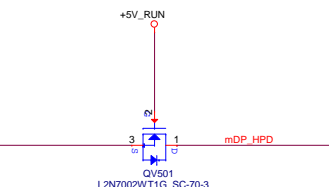
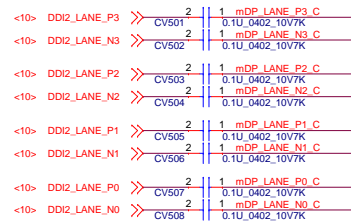
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### AUX/DDC SW for DDI1 to Mini DP



mDP_CA_DET	Function
1	mDP
0	HDMI



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**HDMI CONN**

**LA-A961P**

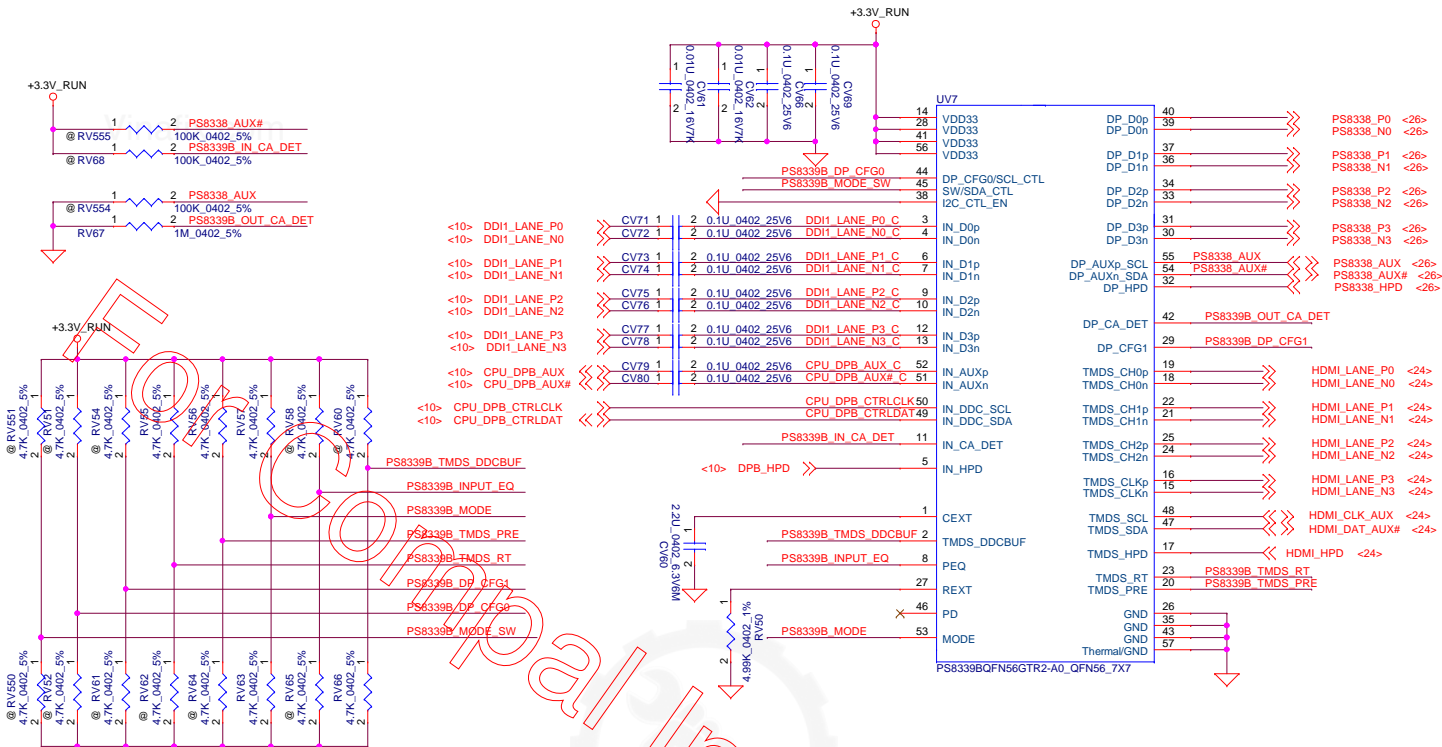
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PCB	DP SWITCH
G12 UMA	PS8339+DP8338
G12 Entry	PS8339
G14 DSC	PS8339+DP8338
G14 UMA	PS8339+DP8338
G14D_En	PS8339
G14U_En	PS8339



MODE = L: Control Switching Mode, HDMI ID disable  
= H: Automatic Switching Mode, HDMI ID disable  
= M: Automatic Switching Mode, HDMI ID enable

TMDS\_PRE = L: no pre-emphasis  
= H: 1.5dB pre-emphasis  
= M: 3.0dB pre-emphasis

TMDS\_RT = L: Standard open drain driver  
= H: Open drain driver with termination resistors

TMDS\_DDCBUF = L: DDC pass through  
= H: DDC active buffer  
= M: DDC pass through with 40 kohm pull up resistor

PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2  
= H: HEQ, compensate channel loss up to 15dB @ HBR2  
= M: LLEQ, compensate channel loss up to 5dB @ HBR2

DP\_CFG1 = L: default, auto test disable & input offset cancellation enable  
= H: auto test enable & input offset cancellation enable  
= M: auto test disable & input offset cancellation disable

DP\_CFG0 = L: default, automatic EQ enable & AUX interception enable  
= H: automatic EQ disable & AUX interception enable  
= M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing

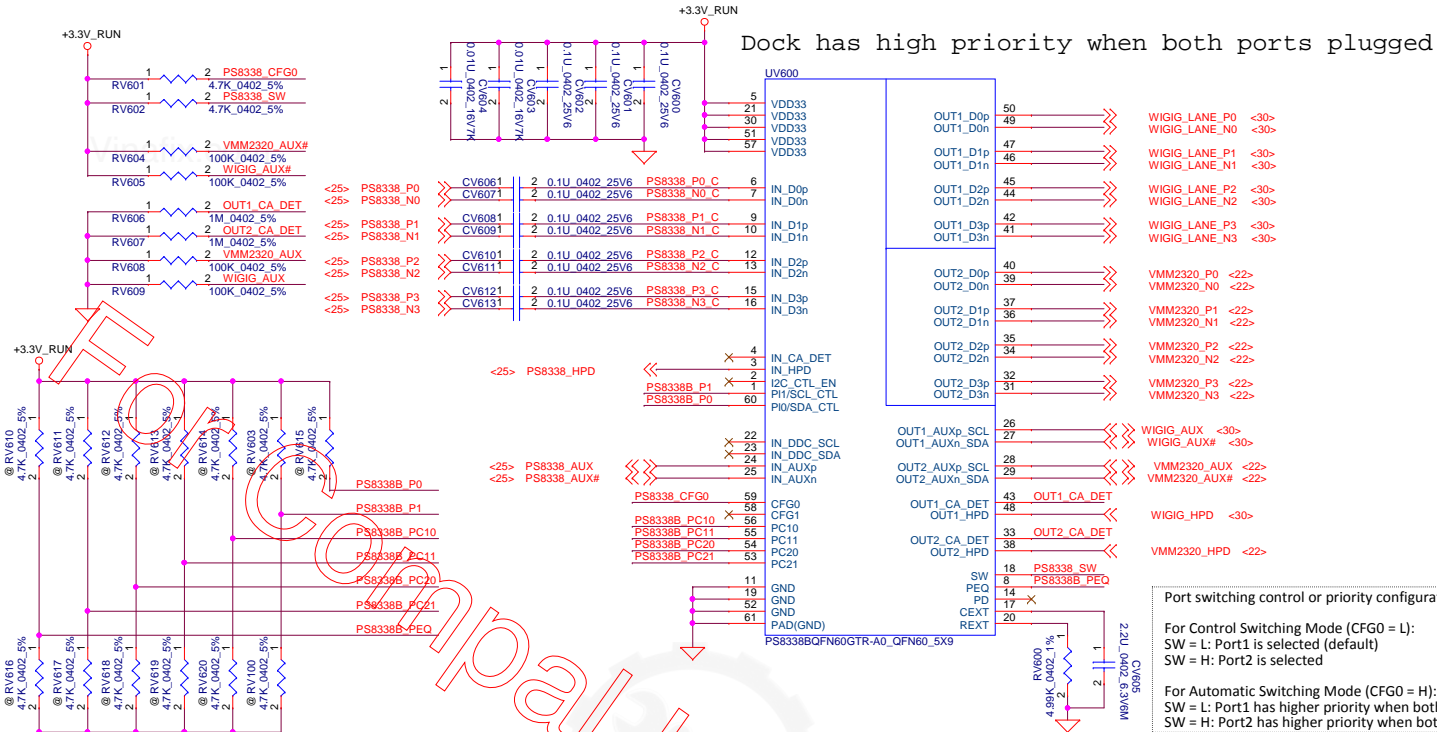
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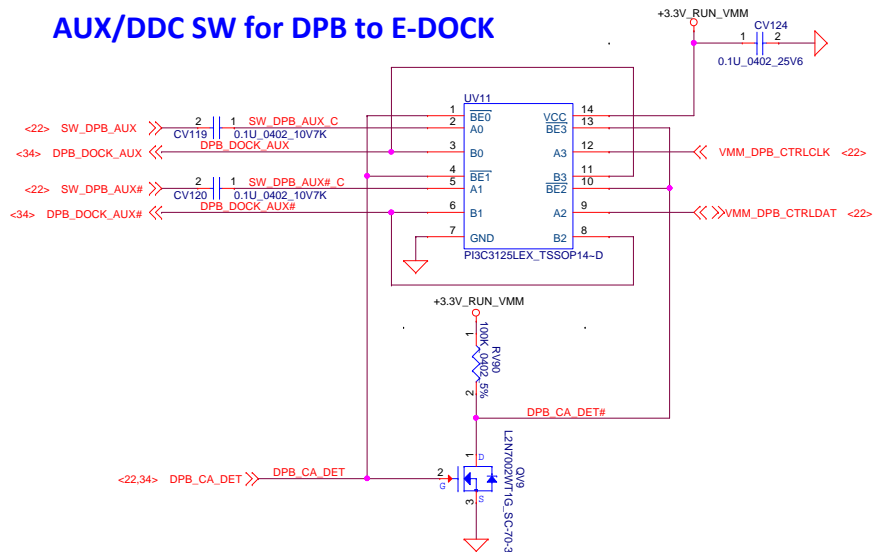


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Title DP SW			
Size	Document Number	Rev	
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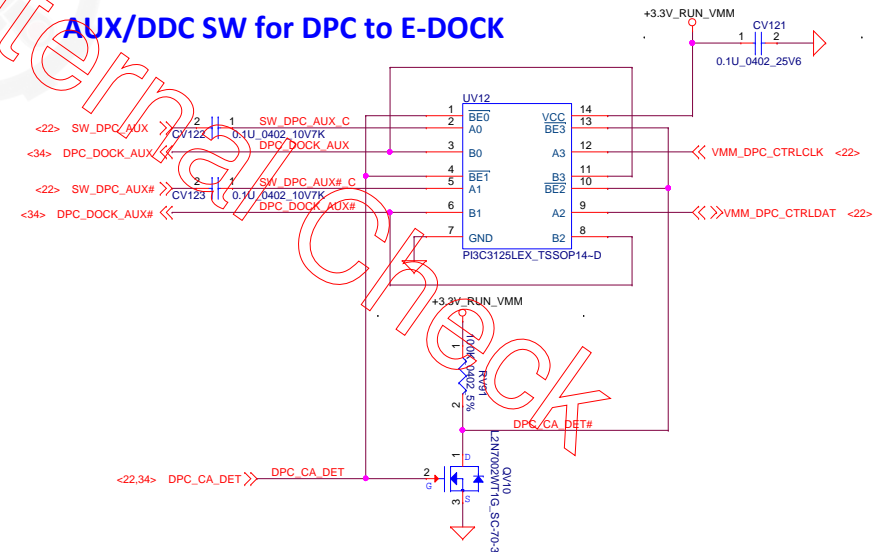
PCB	DP SWITCH
G12 UMA	PS8339+DP8338
G12 Entry	PS8339
G14 DSC	PS8339+DP8338
G14 UMA	PS8339+DP8338
G14D_En	PS8339
G14U_En	PS8339



## AUX/DDC SW for DPB to E-DOCK



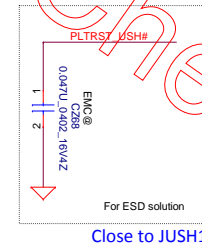
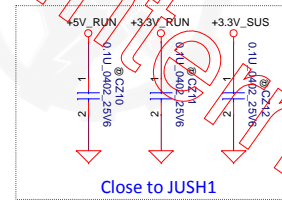
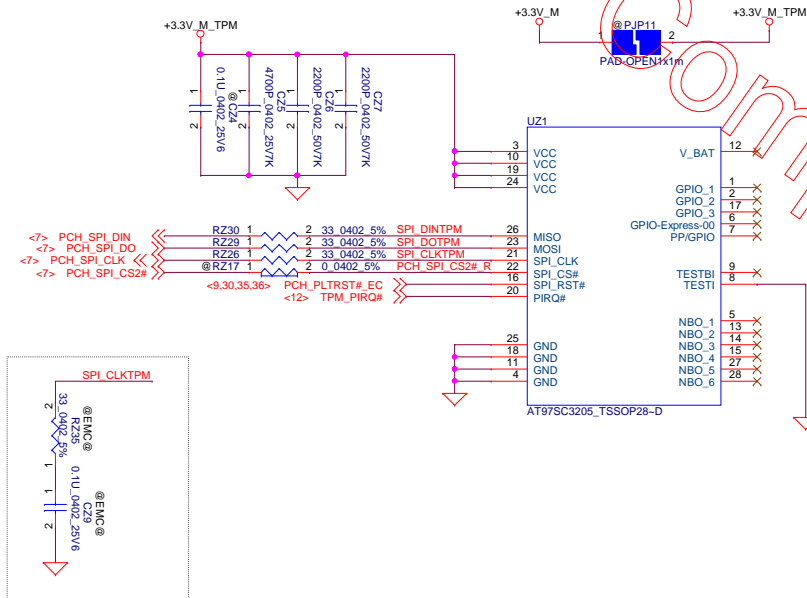
## AUX/DDC SW for DPC to E-DOCK



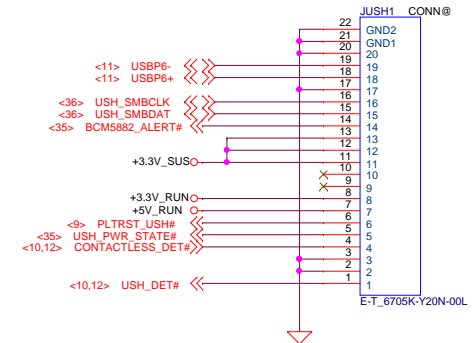
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## USH CONN



20131016 change back to 20pin

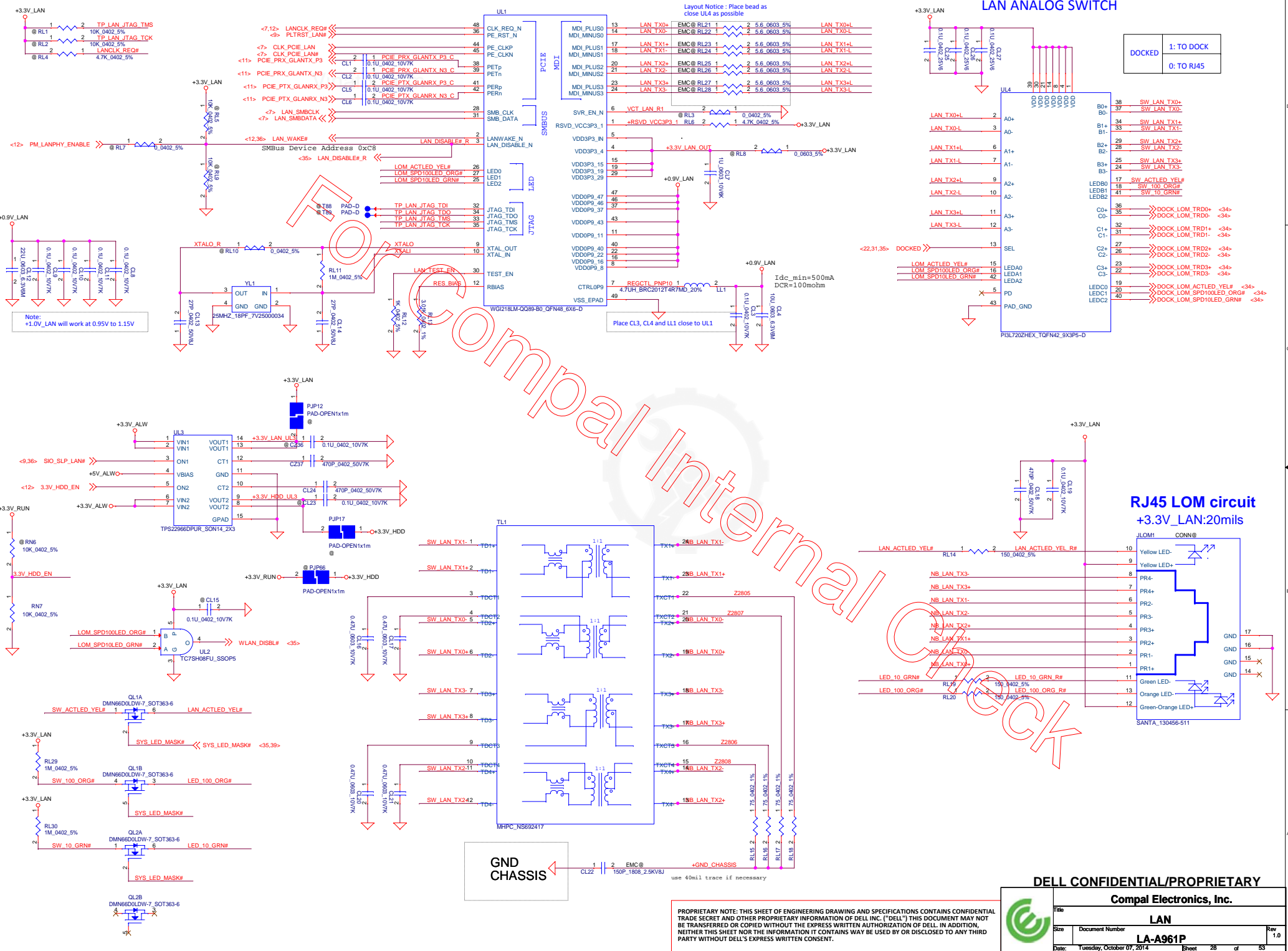
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USH & TPM			
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LAN ANALOG SWITCH

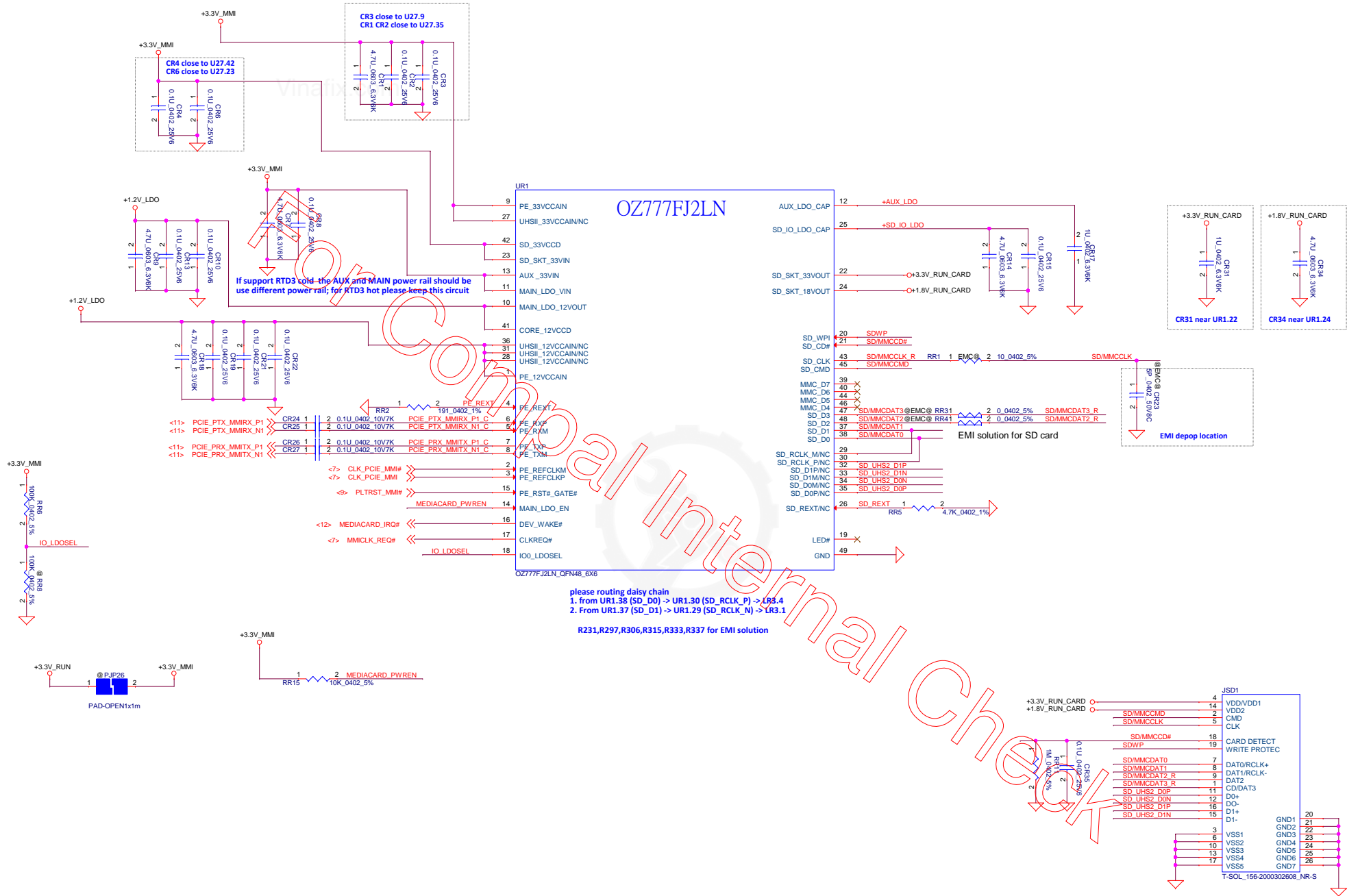
DOCKED	1: TO DOCK
	0: TO RJ45

RJ45 LOM circuit  
+3.3V\_LAN:20mils

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Card Reader

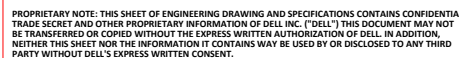
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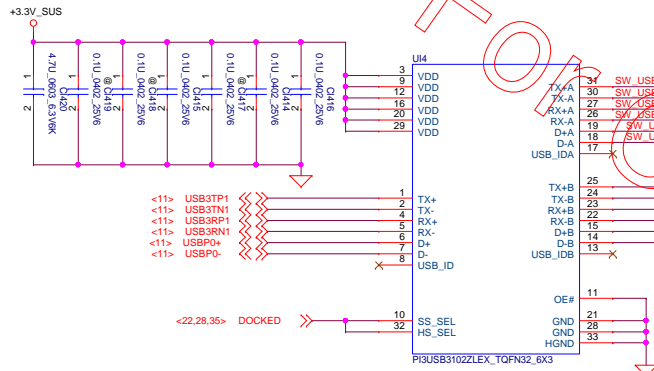
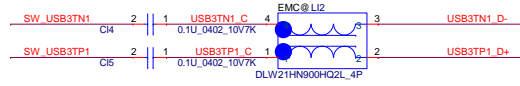
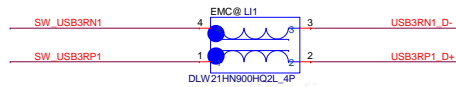
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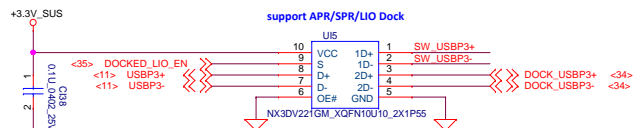
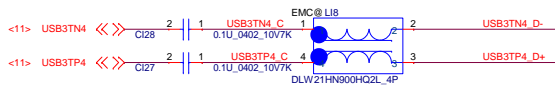
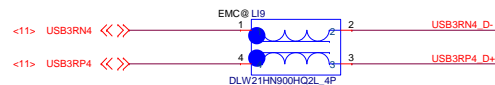






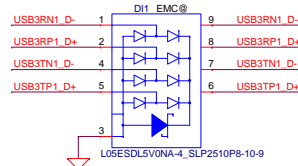
check port mapping

DOCKED	function
1	Dock
0	M/B

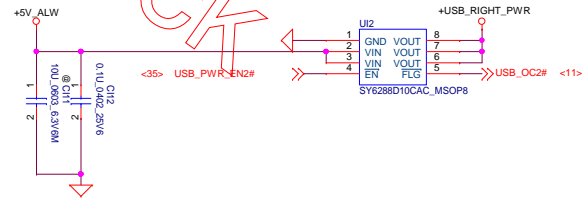
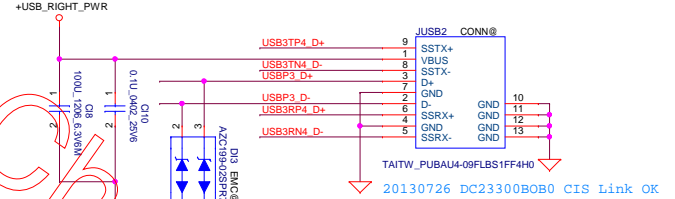
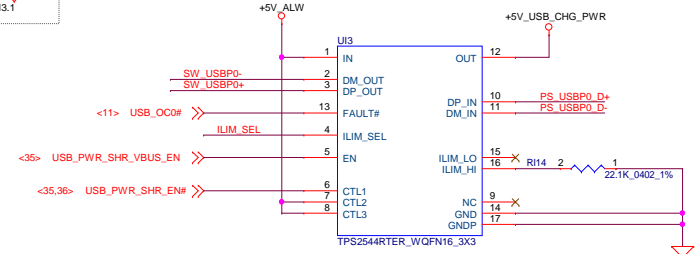
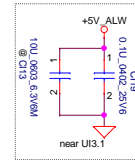
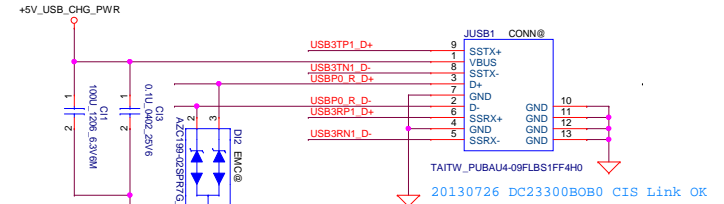
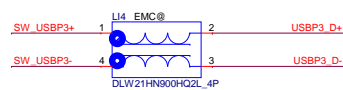
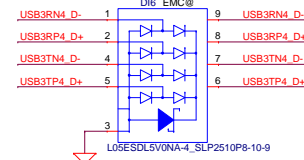


check port mapping

DOCKED_LIO_EN	function
1	Dock
0	M/B



PCB	USB2 0	USB2 3
G12 UMA	USB3102	NX3DV221
G12 Entry	NA	NA
G14 DSC	USB3102	NX3DV221
G14 UMA	USB3102	NX3DV221
G14D En	NA	NA
G14U En	NA	NA



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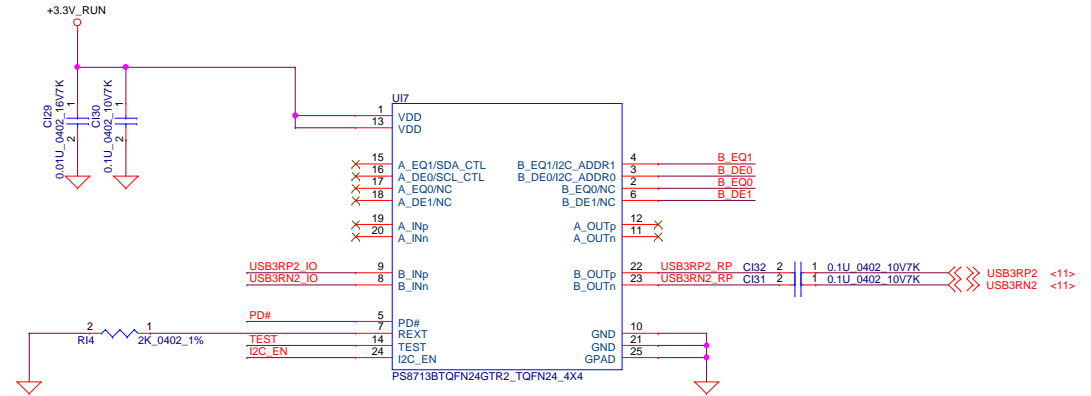
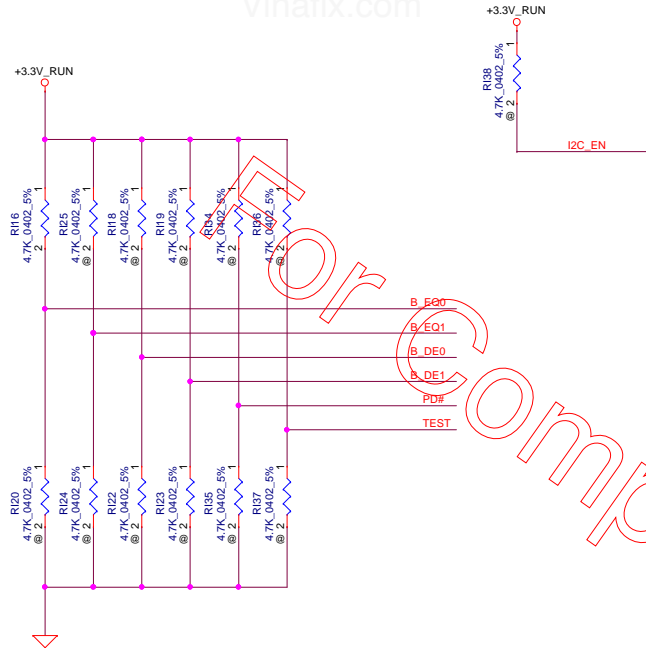
USB3.0

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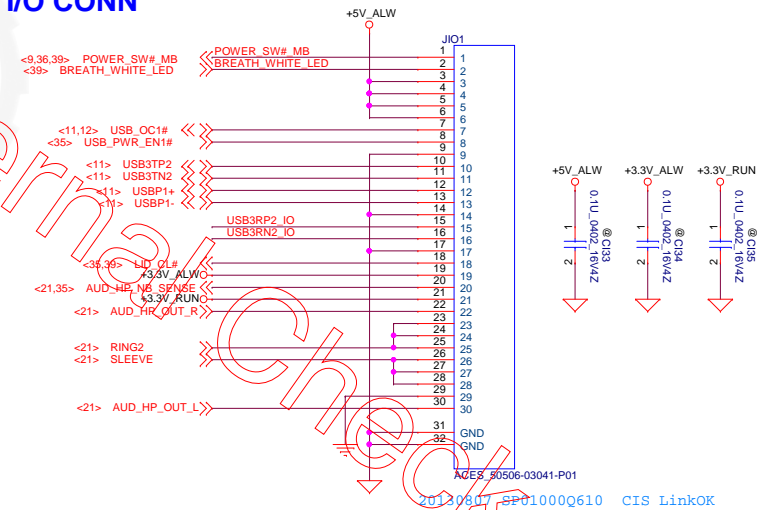
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# USB3.0 repeater

Vinafix.com



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USB SW		
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# NFC on USH/B

For Compal Internal Check

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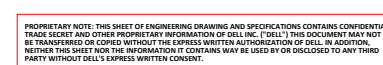


Title		
NFC		
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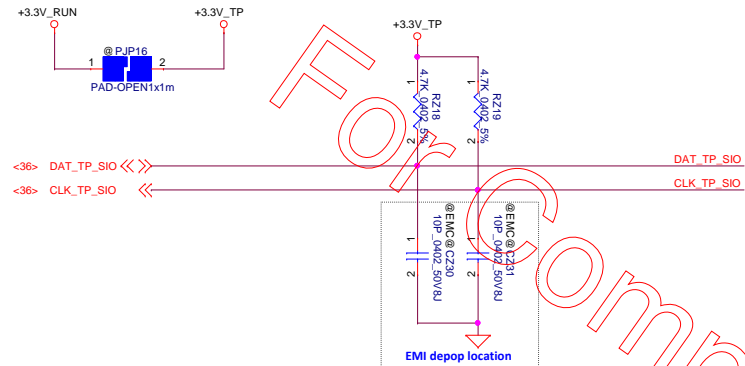




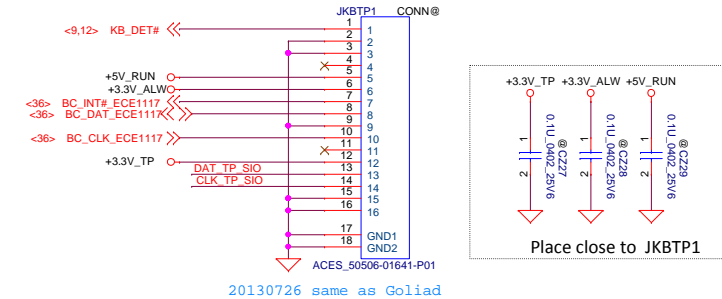




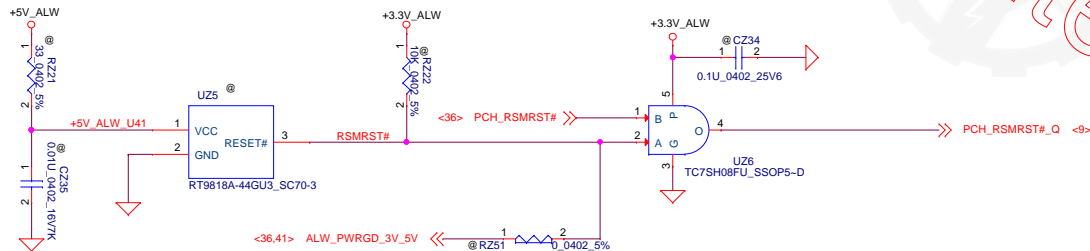
## Touch Pad



## Keyboard



## RSMRST circuit



Part Number	Description
DA30000GZ00	FPC 0VN LF-9591P REV0 M/B-IO/B

Part Number	Description
DC02C004K00	H-CONN SET 0VN MB-LCD-LED-CAM-TS

Part Number	Description
DC02C004K00	H-CONN SET 0VN MB-LCD-LED-CAM

Part Number	Description
DC02C004K00	H-CONN SET 0VN MB-HUB

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

Part Number	Description
NBX0001CW00	FPC 8P G P0.5 PAD0.3 50MM MB-MEDIA/B 0VN

Part Number	Description
NBX0001CZ00	FPC 15P G P.5 PAD.3 85MM MB-NFC MODU 0VN

Part Number	Description
NBX0001CZ00	FPC 15P G P.5 PAD.3 85MM MB-NFC MODU 0VN

Part Number	Description
NBX0001CY00	FPC 20P G P0.5 PAD=0.3 75MM MB-USH/B 0VN

Part Number	Description
NBX0001D100	FPC 6P G P0.5 PAD=0.3 75MM USH/B-FP 0VN

Part Number	Description
FP230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

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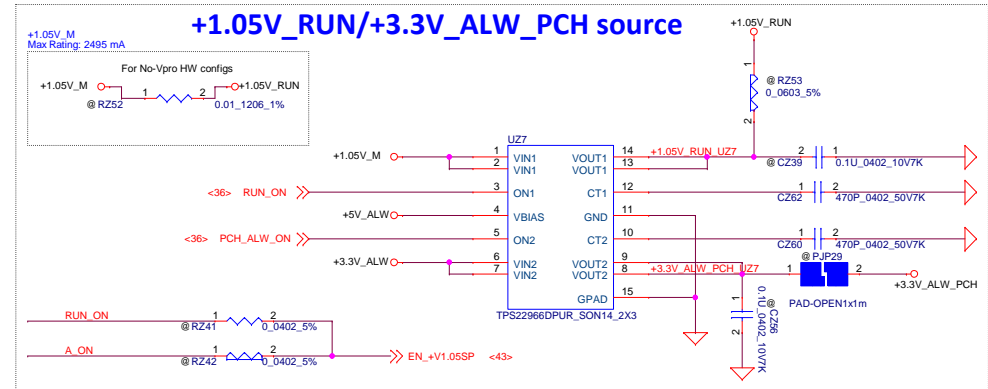
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Title		
Keyboard		
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if support MODPHY off keep DSC solution  
MODPHY timing spec 0.7V/us and <65us

Timing diagram for SATA and PCIe REF/RCOMP, VCCUSBP/L, VCCSATA3P/L. The diagram shows three signals: HSIOPC (black), VCCHSIO (green), and VCCSATA3P/L (blue). HSIOPC is a square wave. VCCHSIO and VCCSATA3P/L are ramps. The ramp for VCCHSIO has a slope of 0.7V/us. The ramp for VCCSATA3P/L has a slope of < 0.1V/us. The time between the start of the ramps is < 65us.



### +3.3V\_M/+3.3V\_SUS source

The diagram illustrates the power supply configuration for the +3.3V\_M/+3.3V\_SUS source. Key components include:

- TPS22966DPUR\_S0N14\_2x3**: A dual-channel voltage translator.
- PJP19 PAD-OPEN1x1m @**: A jumper point for the +3.3V\_SUS source.
- Resistors**:  $R_{240}$ ,  $R_{241}$ ,  $R_{247}$ , and  $R_{246}$ .
- Capacitors**:  $C_{Z40}$ ,  $C_{Z41}$ , and  $C_{Z43}$ .

**Callout Box Details:**

For No-Vpro HW configs


+3.3V\_RUN → [Resistor R246] → +3.3V\_M

Pin values: 0.1U\_0402\_10V7K, 470P\_0402\_50V7K, 0.0603\_5%, 0.1U\_0402\_10V7K.

**+3.3V\_RUN/+5V\_RUN source**

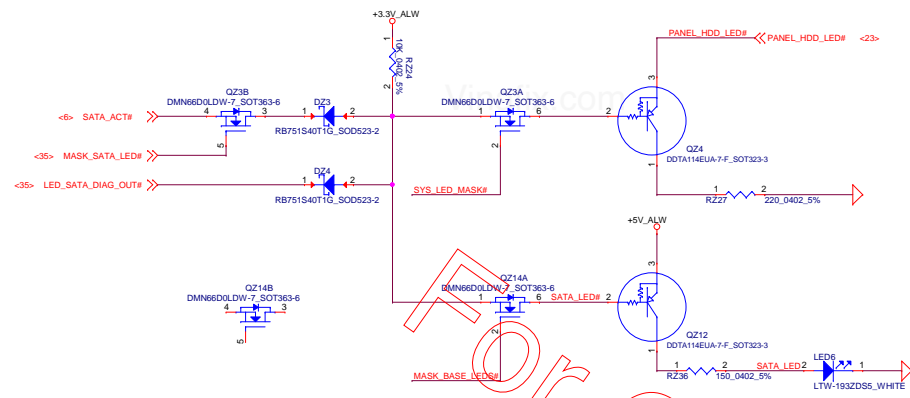
The schematic shows the internal connections of the TPS22966DPUR SGM14-2x5 regulator. Key components and connections include:

- Inputs:** +5V\_ALW and +3.3V\_ALW.
- Outputs:** +5V\_RUN, +3.3V\_RUN.
- Components:** PJP21 PAD-OPEN1x3m, PJP22 PAD-OPEN1x3m, CZ44, CZ45, CZ46, CZ47, UZ9, UZ3.
- Resistors:** 0.1u, 470P, 1000P.
- Capacitors:** CZ44, CZ45, CZ46, CZ47.
- Regulator:** TPS22966DPUR SGM14-2x5.

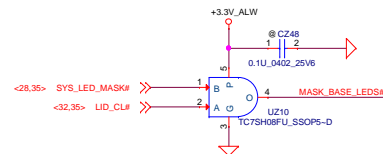
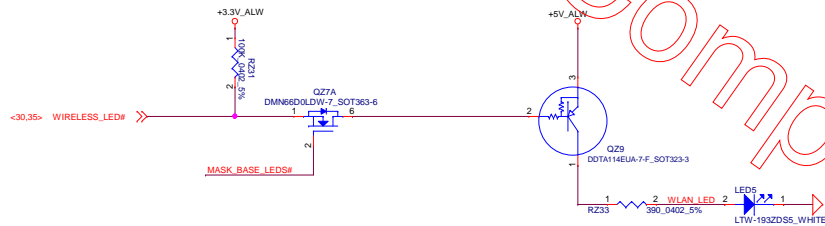
		<b>Compal Electronics, Inc.</b>	
Title		<b>Power control</b>	
Size	Document Number	<b>LA-A961P</b>	Rev 1.0
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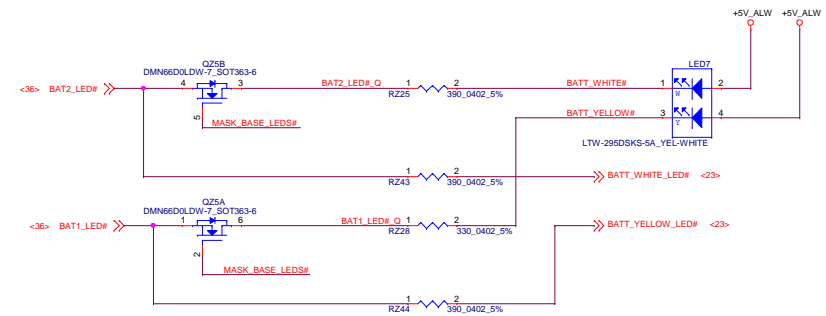
## HDD LED solution for White LED



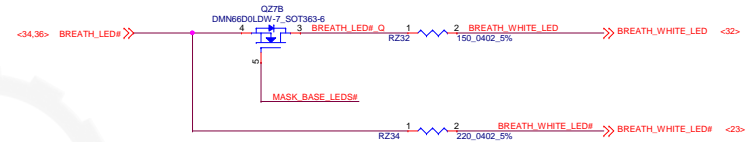
## WLAN LED solution for White LED



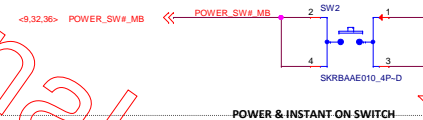
## Battery LED



## Breath LED

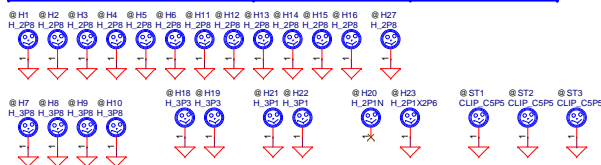


## PWR SW

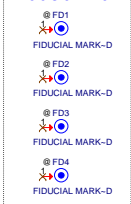


LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



### Fiducial Mark

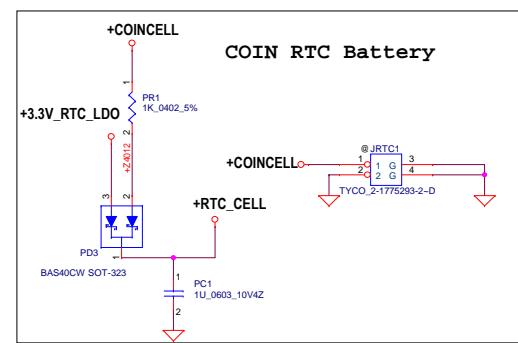
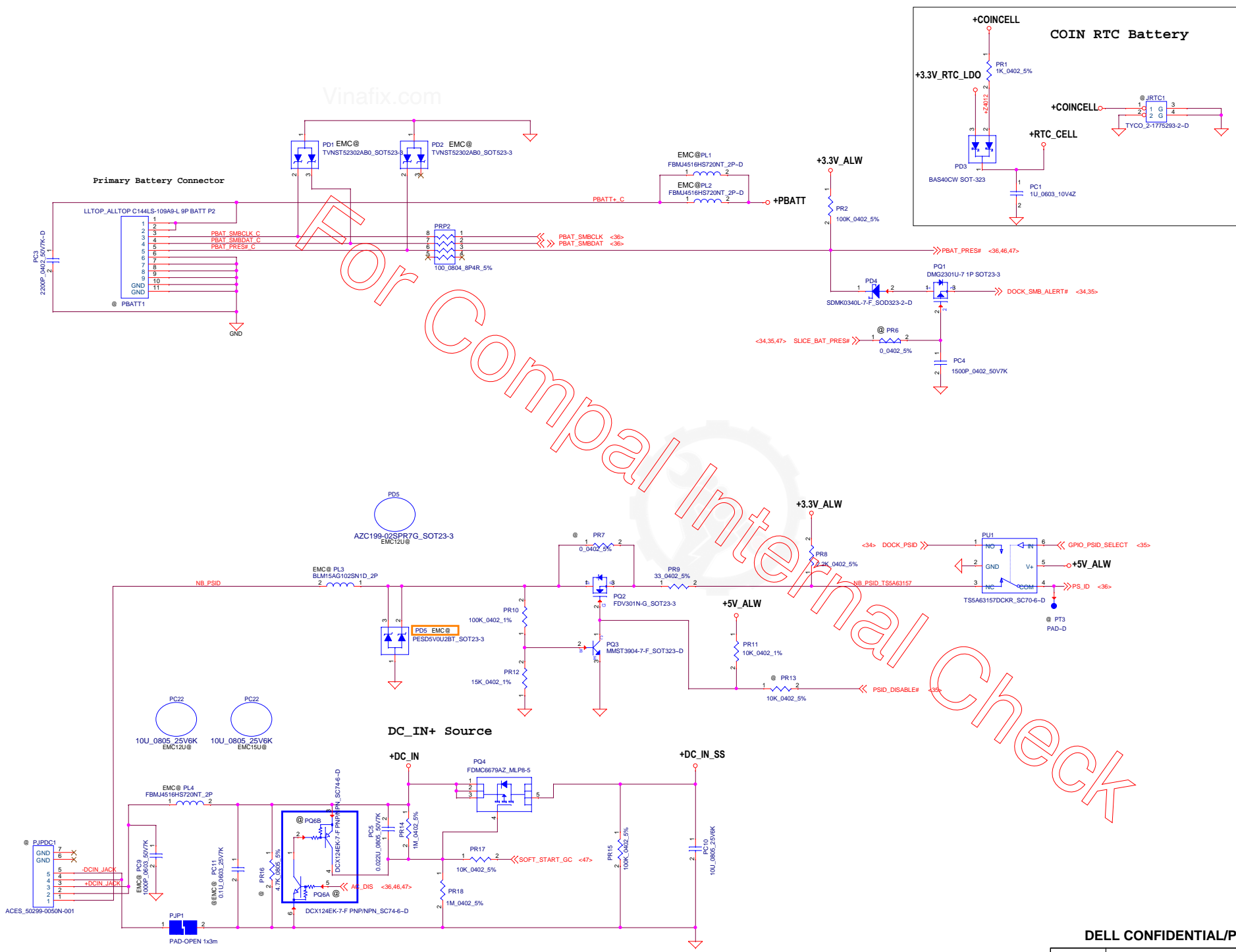


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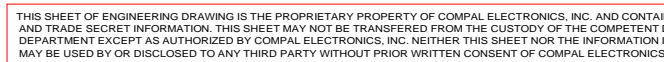
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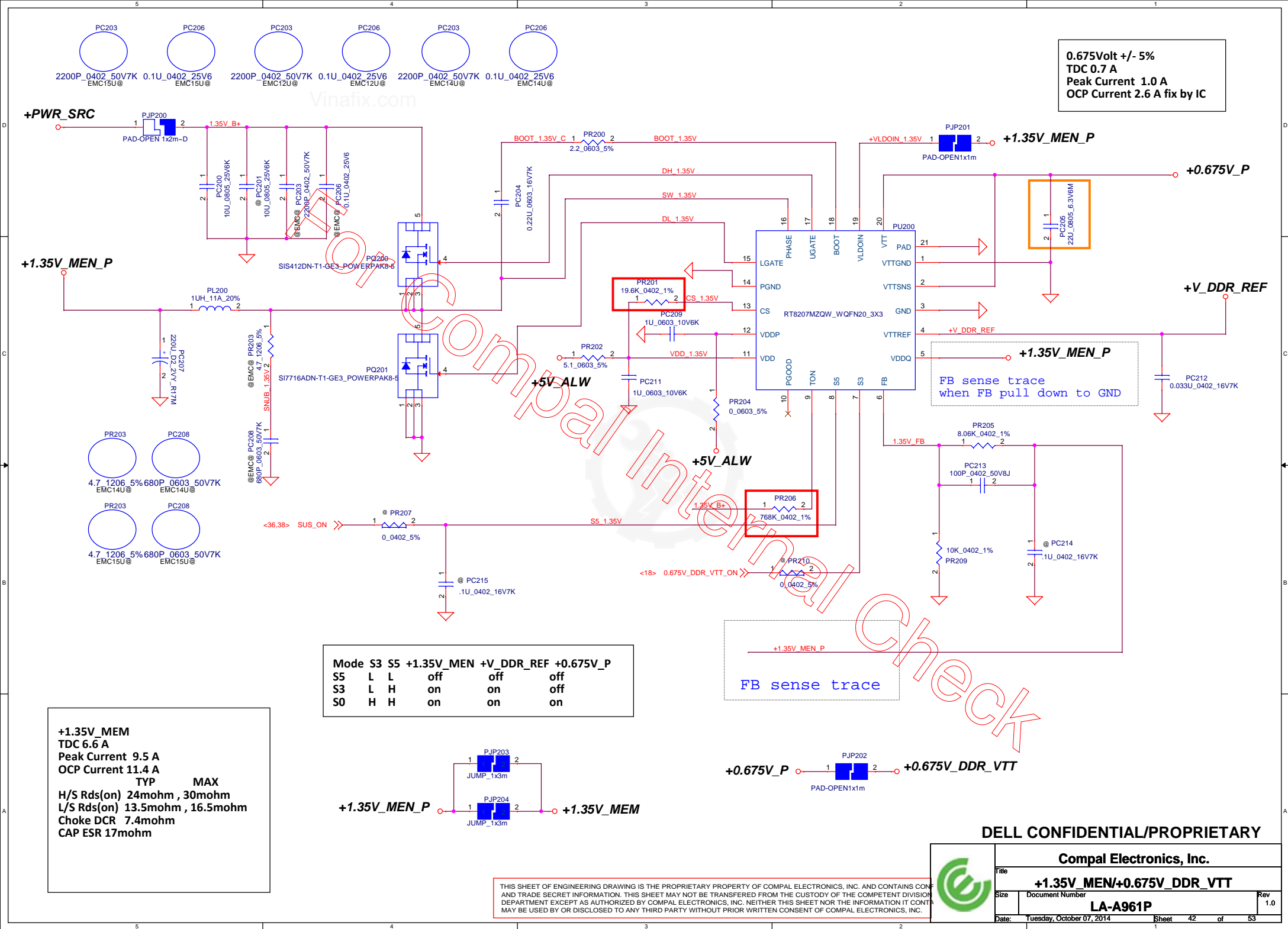


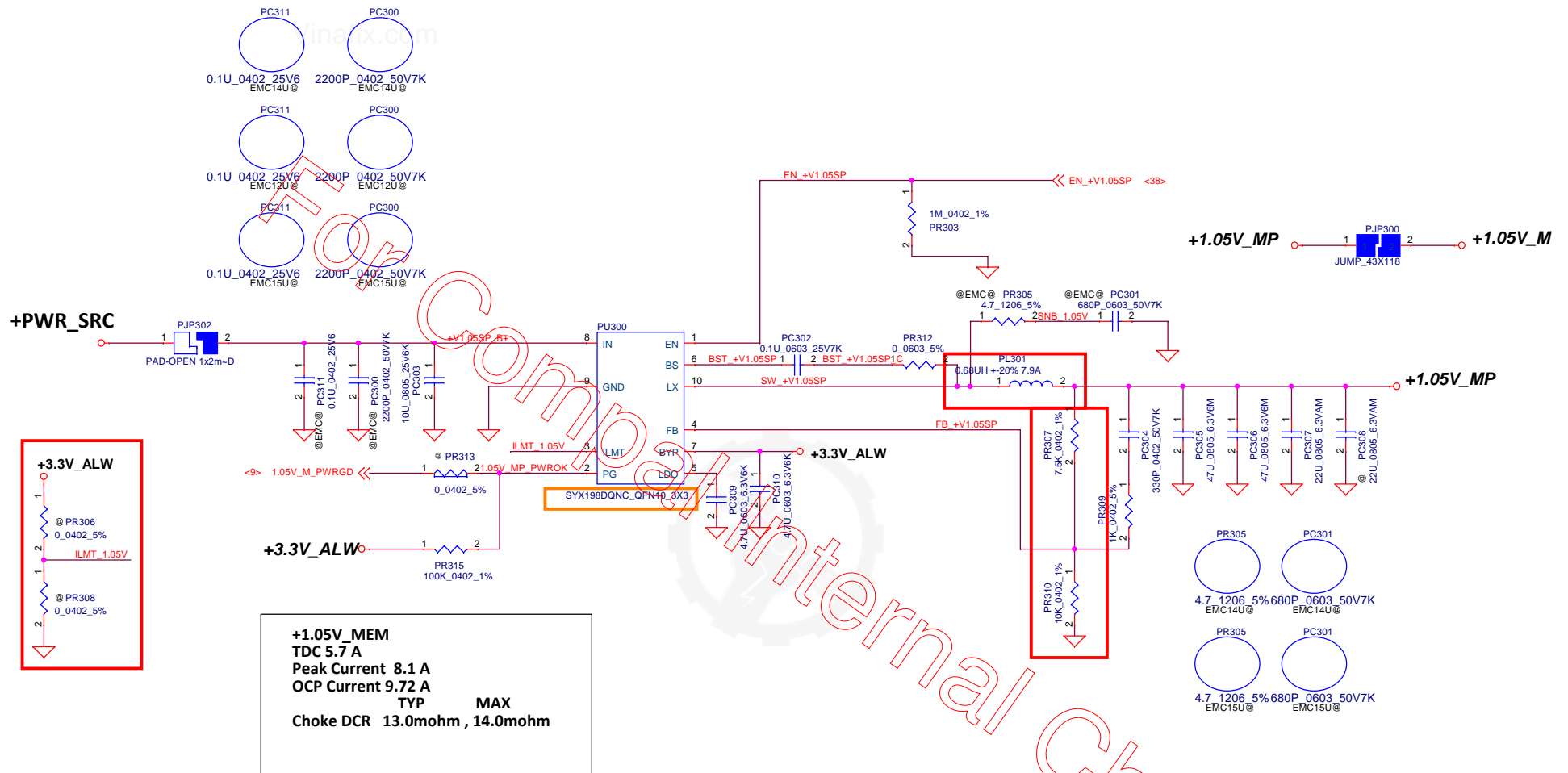
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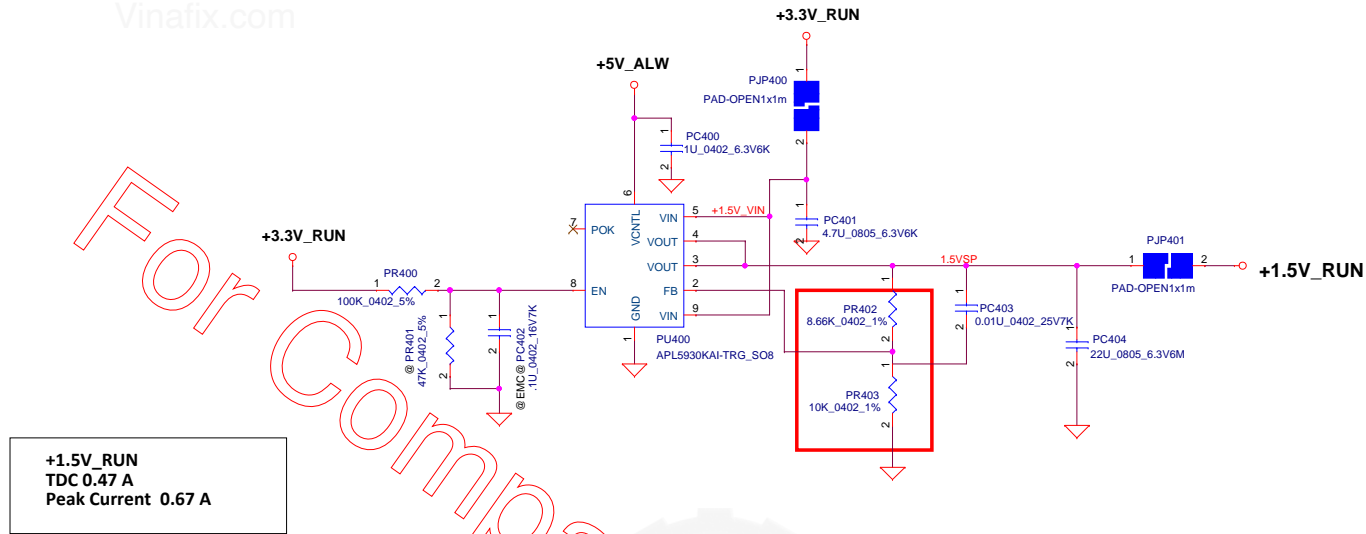


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Title		+1.05V_M	
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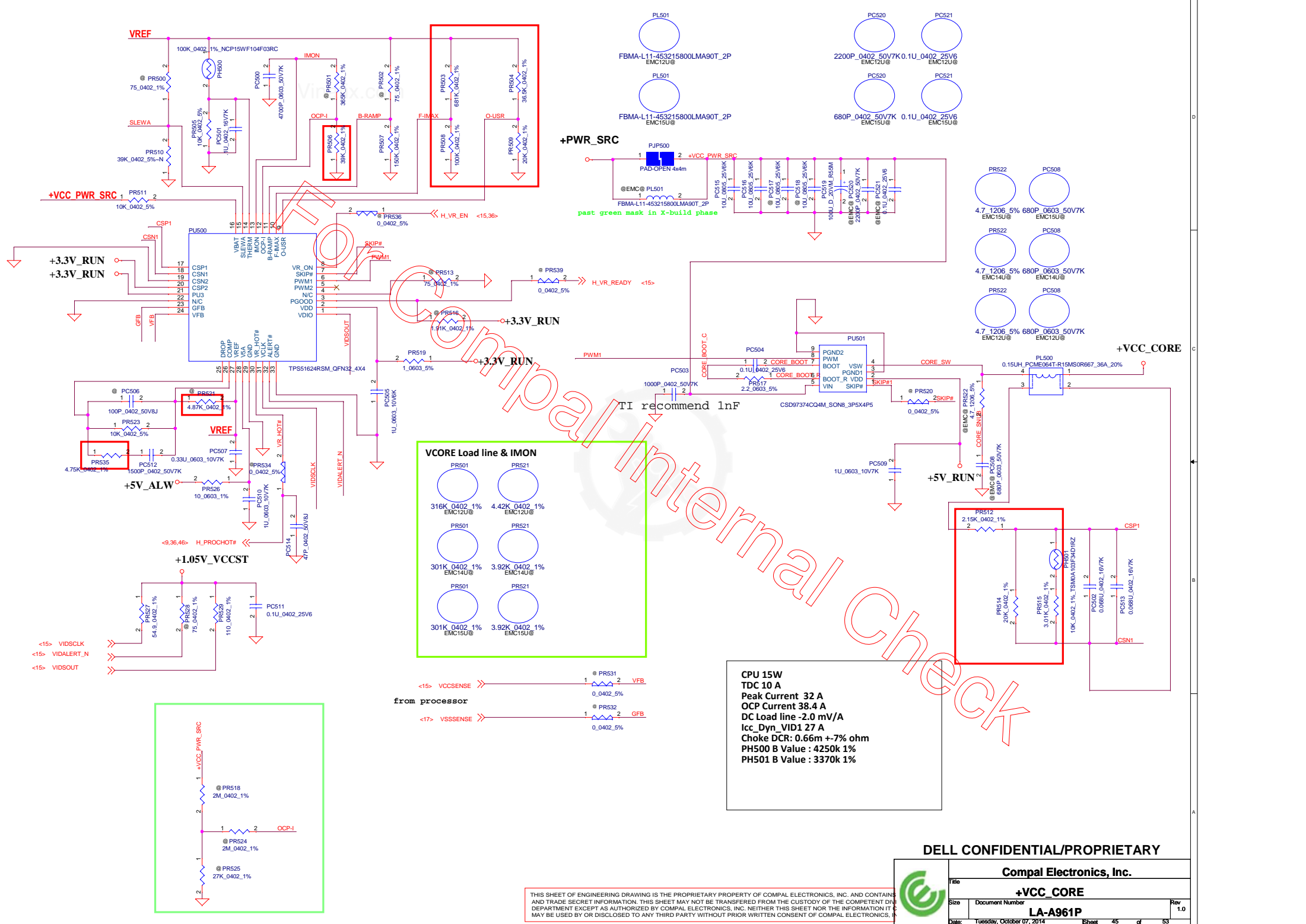




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File	<b>+1.5V_RUN</b>	
Size	Document Number	Rev
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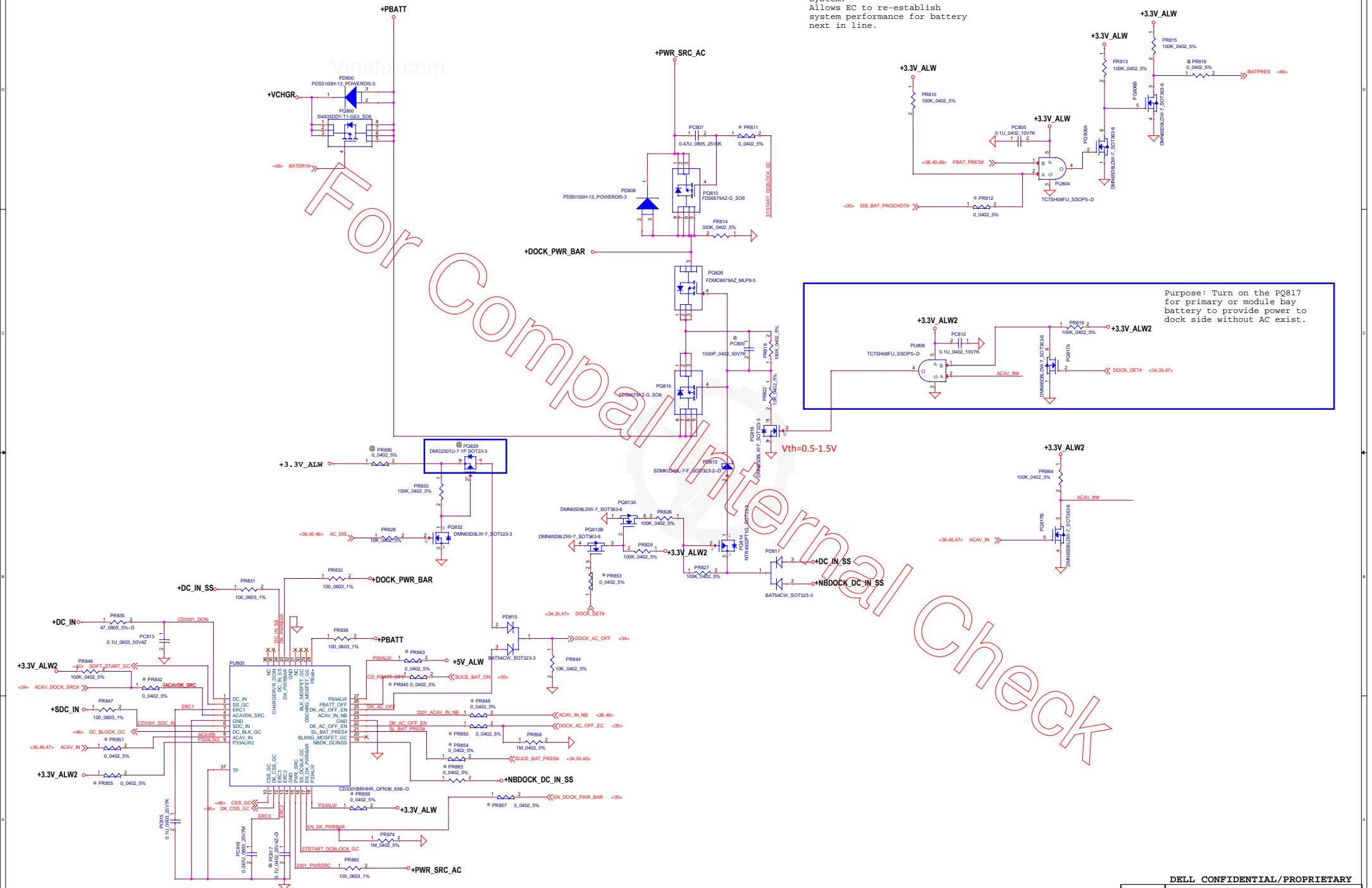


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CPU 15W  
TDC 10 A  
Peak Current 32 A  
OCP Current 38.4 A  
DC Load line -2.0 mV/A  
Icc\_Dyn\_VID1 27 A  
Choke DCR: 0.66m  $\pm$ 7% ohm  
PH500 B Value : 4250k 1%  
PH501 B Value : 3370k 1%



Purpose: Trigger PROCHOT# when active battery is removed from system.  
Allows EC to re-establish system performance for battery next in line.



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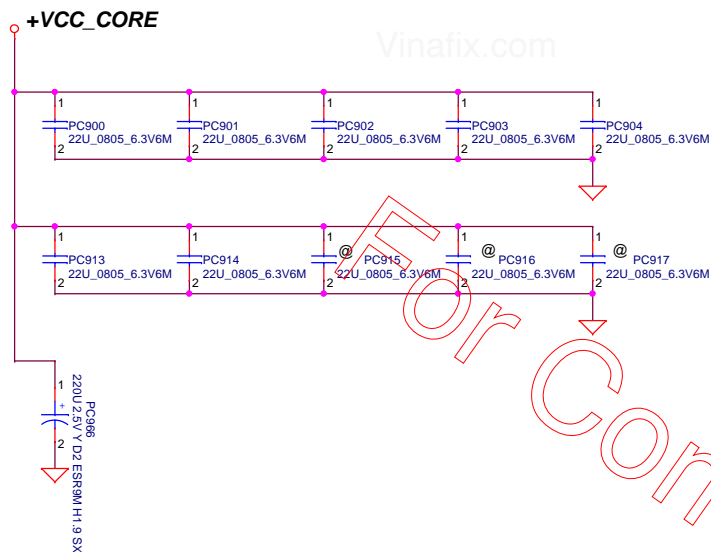
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### Selector

Number **LA-A961P**

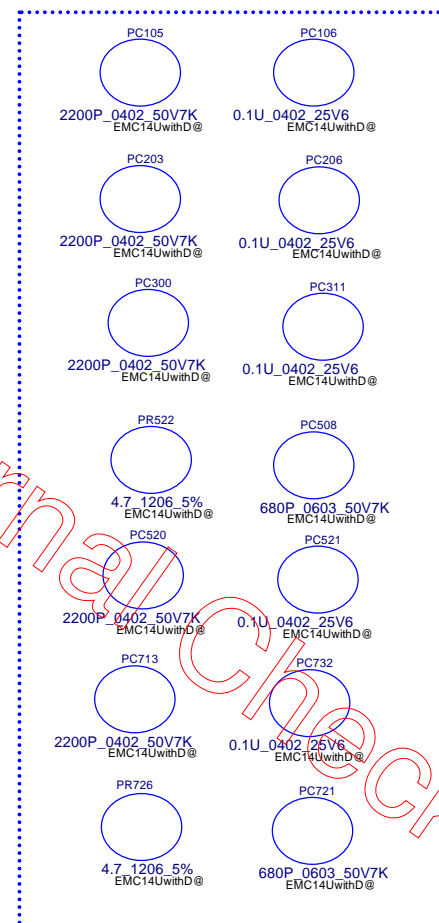
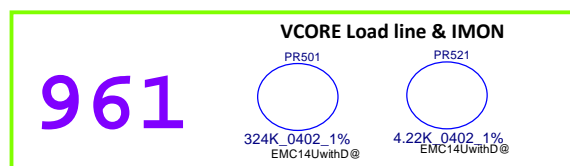
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Based on \_RF Cheng. Hill  
鄭智仁(11257) for PT 20131107

961



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PROCESSOR DECOUPLING

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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	HW	2013/10/16	COMPAL	Follow intel reference circuit.	Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST	0.2(X01)
2	27	HW	2013/10/16	COMPAL	Dell drop POA function.	Change JUSH1 from 26 pin to 20 pin, pin define follow E5	0.2(X01)
3	36	HW	2013/10/16	COMPAL	Dell drop POA function.	remove POA_WAKE# off page symbol remove POA_ON/OFF#,make UE2.B62 to be NC pin	0.2(X01)
4	22	HW	2013/10/16	COMPAL	IC version changed.	VMM2320 circuit change: 1. UV8 from VMM2320 change to VMM 2330 (SA00007G800) 2. UV8 pin J3, E5 to +1.05V_RUN 3. VMM_SPI_WP# reserved RV517, 2.2K resistor PU to +3.3V_RUN_VMM 4. VMM_GPIO4,reserved RV518, 2.2K resistor PU to +3.3V_RUN_VMM 5. VMM_GPIO5 reserved RV519, 2.2K resistor PU to +3.3V_RUN_VMM 6. UV8 pin B5, B6 change to +3.3V_RUN_VMM 7. LP_CTL reserved RV516, 2.2K resistor PU to +3.3V_RUN_VMM 8. Depop RV73	0.2(X01)
5	36	HW	2013/10/16	COMPAL	board ID change.	RE79 change to 130K	0.2(X01)
6	36	HW	2013/10/16	COMPAL	follow intel latest design guide.	pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor	0.2(X01)
7	9	HW	2013/10/16	COMPAL	HDMI circuit issue	swap TMDS_CON_P/N2 & TMDS_CON_P/N0	0.2(X01)
8	7	HW	2013/10/20	COMPAL	RF requirement.	add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)	0.2(X01)
9	38	HW	2013/10/20	COMPAL	power doesn't split VPRO & NPRO BOM.	add RZ41, RZ42, reserve it for VPRO & NVPRO option.	0.2(X01)
10	28	HW	2013/10/20	COMPAL	SSI design will cause LED behavior error.	ChangeQL1,QL2 MASK_BASE_LEDS# to SYS_LED_MASK#	0.2(X01)
11	30	HW	2013/10/22	COMPAL	To solve Line-on HDD dirty shut down issue.	Add RN6,RN7 and reserved RN7	0.2(X01)
12	6	HW	2013/10/23	COMPAL	debug usage.	add RC301	0.2(X01)
13	6, 7, 22, 28	HW	2013/10/23	COMPAL	follow xtal vender suggest	1 CC1 &CC2 change from 18PF to 5PF 2 CC8 & CC11 change from 18PF to 15PF 3 CL13 & CL14 change from 33PF to 27PF 4 RV81 change from 0 ohm to 2.2K & CV113 change to 18PF	0.2(X01)
14	9	HW	2013/10/30	COMPAL	reserve it to prevent PCH_PLTRST# floating when power on	add RC304, 100K pull down, on PCH_PLTRST#_EC	0.2(X01)
15	12	HW	2013/10/30	COMPAL	To solve backdrive issue.	Change TPM_PIRQ# pull up ( RC247) to +3.3V_RUN from +3.3V_ALW_PCH	0.2(X01)
16	38	HW	2013/10/30	COMPAL	No support MODPHY	add PJP36, depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.2(X01)

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17	32	HW	2013/11/2	COMPAL	USB3.0 EA finetune	Pop RI2	0.2(X01)
18	25	HW	2013/11/2	COMPAL	HDMI EA finetune	Pop RV55,RV62	0.2(X01)
19	37	HW	2013/11/2	COMPAL	Dell request.	add RZ48, RZ49, QZ15 depop UZ5, UZ6, RZ21, RZ22, CZ35,RC91 add RZ51, change QZ12 from 3904 to 3906. make RPE6 to be NC pin, add RE88	0.2(X01)
20	36	HW	2013/11/6	COMPAL	Dell request	1 pop RE282, depop RE281. change SUS_ON control pin from SUS_ON_EC to SIO_SLP_S4# 2 change RC91, RE88 from 10K to 47K	0.2(X01)
21	12	HW	2013/11/6	COMPAL	UMA Dock has one dimm config	add DIMM_DET on UC1.U48 to replace PCH_GPIO48 ,Reserve RC302 &RC303	0.2(X01)
22	38	HW	2013/11/6	COMPAL	UMA Dock has VPRO & N-VPRO config	change PJP18 to RZ53 ,PJP19 to RZ47 for VPRO config Add RZ52,RZ46 for NVPRO config	0.2(X01)
23	25	HW	2013/11/6	COMPAL	follow vender suggest to solve "Bo" noise	1.UA1 pin22 add RA45 0 ohm PU to +3.3V_RUN_AUDIO 2.UA1 pin21 add RA44 100k ohm to GND	0.2(X01)
24	22	HW	2013/11/6	COMPAL	follow vender suggest	1.RPC8 change from 2.2k to 10k 2.UC1.F2 &RPC8.3 change name from I2C0_SDA to PCH_GPIO4 3.UC1.F3 &RPC8.4 change name from I2C0_SCL to PCH_GPIO5 4.UC1.G4 &RPC8.1 change name from I2C1_SDA_VMM to PCH_GPIO6 5.UC1.F1 &RPC8.2 change name from I2C1_SCL_VMM to PCH_GPIO7 6.RPV2.1 connect to I2C1_SDA_VMM 8.RPV2.2 connect to I2C1_SCL_VMM 9.Depop RV516, CV116, CV117	0.2(X01)
25	22	HW	2013/11/6	COMPAL	To solve CRT display jitter issue	1.LV23,LV25 change from BLM15AX102SN1D to BLM15PX181SN1D 2.CV90,CV101 change from 1uF to 10uF	0.2(X01)
26	37	HW	2013/11/6	COMPAL	Base on Pre-PT RSMRST EA result	1.POP RE88,UZ6,RE51 2. remove QZ12,RZ48,RZ49,RZ50	0.2(X01)
27	22	HW	2013/11/6	COMPAL	follow vender suggestion	1. change LV22 , LV24 From SM01000N400 S SUPPRE_MURATA_BLM15AX102SN1D 0402 To SM01000NO00 S SUPPRE_MURATA_BLM15PX181SN1D 0402 2. change CV82, CV94 from 1uF to 10uF 3. UV8 pin D3 from +1.05V_VMM_VDDTX to +1.05V_VMM_VDD. 4. UV8 Pin H3, E10, H11 change to NC 5. Change UV8 pin B5, B6 from +3.3V_RUN_VMM to +3.3V_RUN_VDDIO"	0.2(X01)
28	30	HW	2013/11/6	COMPAL	Support New NFC module	Pop R2,R3 & Remove PJP50	0.2(X01)

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29	32	HW	2013/11/6	COMPAL	follow vender suggestion	RA7,RA8 change to 24.9ohm	0.2(X01)
30	36	HW	2013/11/6	COMPAL	For Delray EC common code GPIO definition different	Add RE283 to separate EC and ALW_PWRGD_3V_5V	0.2(X01)
31	38	HW	2014/02/06	COMPAL	For MODPHY power rail contril by JUMP directly	1.change PJP36 pin1 from +1.05V_M to +1.05V_RUN	0.3(X01)
32	25	HW	2014/02/10	COMPAL	Base on PS8338 datasheet, PI0 have 2 level, PII have 3 level	For PI0, delete RV66 For PII, add RV100 PD to GND	0.3(X01)
33	32	HW	2014/02/24	COMPAL	USB3.0 repeator	Change USB3.0 repeator from PS8711 to PS8713	0.3(X01)
34	33	HW	2014/03/06	COMPAL	Remove NFC Funciton	Remove NFC circuit 1.remove RC221 2.remove Q1,Q2,U1,R1,R2,R3,C1,C2,C3,C4,C5,RC36,RC37,RC246 3.NC PCH_GPIO28 ; PCH_GPIO70 4.net name PCH_GPIO59 instead of NFC_DET#	0.3(X01)
35	29	HW	2014/03/06	COMPAL	EMI test fail , back to SSI SD card connector.	change JSD1 from ALPS_SCDADA0101_19P_NR to TAITW_PSDCT6-20GLBS1NN4H_19P-T	0.3(X01)
36	9,16	HW	2014/03/06	COMPAL	follow intel DG 1.2	1.reserved 0.47uF for +PCH_VCCDSW3_3 , near CPU AH10 pin 2.add 10K pull high to +PCH_VCCDSW3_3 for PM_LANPHY_ENABLE, leave RPC1. pin 7 NC	0.3(X01)
37	30	HW	2014/03/06	COMPAL	intel Wigig need 32K clock when DSx	1.Add UZ11&RZ56(@)&RZ57 2.JNGFF1.44 change to WIGIG_32KHZ from SUSCLK 3.JNGFF2.60 change to NC from SUSCL	0.3(X01)
38	34	HW	2014/03/06	COMPAL	To solve Power leakage issue.	Change R272 from 10K to 100K, and pull up to +3.3V_ALW2	0.3(X01)
39	9	HW	2014/05/09	COMPAL	XDP config use	CFG3 add RC305 1k PD	0.4(X02)
40	30,38	HW	2014/05/09	COMPAL	reduce 0 ohm quantity	RC50,RZ42,RZ57,RZ47,RZ53 ,RE283 change to 0-ohm short	0.4(X02)
41	9,27	HW	2014/05/09	COMPAL	ESD request	ADD CZ68,CC101	0.4(X02)
42	36	HW	2014/05/19	COMPAL	DVT2.0 Board ID	RE79 change from 130K to 33K	0.4(X02)
43	28	HW	2014/06/09	COMPAL	WLAN can't recognize during enable Unobtrusive mode(Fn+B)	Add RL29,RL30 1M PU add on SW_100_ORG# & SW_10_GRN#	0.4(X02)
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1	47	Selector	10/8	Compal	Remove slice battery support circuit	Remove PC808, PC811, PC812, PC814, PD806, PD807, PD811, PD814, PD819, PD821, PQ801, PQ807, PQ809, PQ811, PQ812, PQ818, PQ821, PQ828, PQ830, PQ831, PR802, PR804, PR808, PR813, PR815, PR816, PR817, PR821, PR823, PR825, PR834, PR836, PR837, PR839, PR849, PR852, PR861, PU805, PU807, PU808	X01
2	45	VCC_CORE	10/8	Compal	To prevent acoustic noise issue	Remove PC923, PC924, PC925, PC926, PC927, PC928, PC929, PC930, PC931, PC940, PC941, PC943, PC946, PC947, PC948 Add PC966	X01
3	42	1.35V_MEN	10/8	RICHTEK	To prevent IC damage	Add PR204	X01
4	46	Charger	10/8	Compal	Fine tune divider voltage	Change PR713, PR725 to 100k Change PR715, PR729 to 154k	X01
5	41,43,44	+1.05V_M +1.5V_RUN +3V/+5V	10/22	Compal	To improve the ability of anti-noise	Change PR307 to 7.5k Change PR310, PR102, PR104, PR403 to 10k Change PR100 to 6.49k Change PR101 to 15k Change PR402 to 8.66k	X01
6	46	Charger	10/25	Compal	Change /BATPRES pin control net from /BATPRES to PBAT_PRES#	Pop PR728 Depop PR816	X01
7	45	VCC_CORE	10/31	Compal	Fine tune IMON	Add PR518, PR524, PR525	X01
8	ALL	ALL	10/31	Compal	RF request	Add PC521, PC206, PC106, PC311, PC732 ( 0.1uF )	X01
9	ALL	ALL	10/31	Compal	RF request	Pop PR111, PC111, PR112, PC114, PR203, PC208, PR305, PC301, PR522, PC508, (4.7ohm, 680pF)	X01
10	46	Charger	10/31	Compal	To prevent VCP trigger PROCHOT#	PR703 change to 100ohm	X01
11	46	Charger	6/26	Compal	For peak power shifting, to avoid back to back turn on to O slowly when battery remove.	1)depop PQ6 2)new add PQ712, Drain connect to ACAV_IN 3)depop PQ829	X03
12	46	Charger	7/7	Compal	for decrease audible noise, Use charger BQ24777 PG2.0 with work around of 3.3uH inductor, and alignment with Houston, so add 2*10uF caps in PC706, PC707	1) PL701 change from 2.2U to 3.3u from (SH00000YF00) S COIL 2.2UH +-20% 12A 10X10X4 MOLDING to (SH00000IC00) S COIL 3.3UH +-20% PLMB104T-3R3MS 10A to  2) add 0805 MLCC in PC706, PC707 (SE00000QK00) S CER CAP 10U 25V K X5R 0805 H1.25	X03
13	40 41	+DCIN +3V/+5V	7/10	Compal	EMI requirement: Please help to pop PD5, PC119(1uF) to implement in DVT2.0 BOM.	Pop 1)PD5 P/N:(SC600001600) S DIO ROW AZC199-02S.R7G C/C SOT23 ESD 2)PC119 P/N:(SE080105K80) S CER CAP 1U 10V K X5R 0603	X03
14	40	+DCIN	2014 /9/26	Compal	follow Houston/ EMI requirement: remove main source (AMC) (SC600001600) S DIO ROW AZC199-02S.R7G C/C SOT23 ESD to avoid negative spike to damage PD5	Change from (SC600001600) S DIO ROW AZC199-02S.R7G C/C SOT23 ESD to (SCA00000T00) S ZEN ROW PESD5V0U2BT 3P C/C SOT23 ESD 註記(H=1.1mm)	A00 DELL CONFIDENTIAL/PROPRIETARY Compal Electronics, Inc. PWR P.I.R (1/1) LA-A961P Date: Tuesday, October 07, 2014 Sheet 53 of 53

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